

Ratchet-1 WHL SVT Logic Schematics

RT1WL-3
VER 3.12
April/1/2019

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BASE LOGIC :

Ratchet-1 WHL SIT Logic Schematic Ver 2.18

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75.DC/DC VCC5M (NB690)
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78.BLANK
79.DC/DC IMVP8 (MP2979AGQKT)
80.DC/DC VCCCPUCORE (MP86941 X 2)
81.BLANK
82.DC/DC VCCGFXCORE_I (MP86901C)
83.DC/DC VCCSA (MP86901A)
84.BLANK
85.DC/DC VCCCPUIO(NB692)
86.DC/DC VCC1R05_SUS (NB692)
87.LOAD SW VCCST & VCCSTG
88.DC/DC VCC1R2A/0R6B/1R8A (NB688)
89.LOAD SW VCCPLL_OC
90.DC/DC VCC1R8_SUS (MP1603L)
91.DC/DC VCCPCHCORE(NB692)
92.BLANK
93.LOAD SW PCH SUS
94.LOAD SW LAN
95.LOAD SW B
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Project Name : Ratchet-1	Title : TITLE PAGE	
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EC HISTORY

RT1IL-3

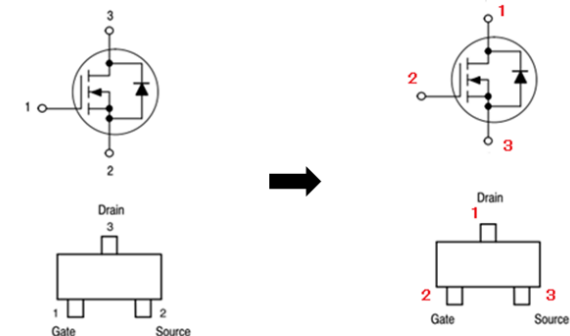
(Base Logic : Ratchet-1 WHL SIT Logic Schematic Ver. 2.18)

VER.3.00 2019/02/18 APPLIED Ratchet-1 SVT EC001,EC002
VER.3.01 2019/02/19 APPLIED Ratchet-1 SVT EC003
VER.3.02 2019/02/20 APPLIED Ratchet-1 SVT EC004,EC005
VER.3.03 2019/02/21 APPLIED Ratchet-1 SVT EC006,EC007,EC008,EC009,EC010
VER.3.04 2019/02/22 APPLIED Ratchet-1 SVT EC011
VER.3.05 2019/02/25 APPLIED Ratchet-1 SVT EC012,EC013
VER.3.06 2019/02/27 APPLIED Ratchet-1 SVT EC014,EC015
VER.3.07 2019/03/04 APPLIED Ratchet-1 SVT EC016,EC017,EC018
VER.3.08 2019/03/13 APPLIED Ratchet-1 SVT EC019,EC020
VER.3.09 2019/03/14 APPLIED Ratchet-1 SVT EC021
VER.3.10 2019/03/15 APPLIED Ratchet-1 SVT EC022,EC023
VER.3.11 2019/03/20 APPLIED Ratchet-1 SVT EC024
VER.3.12 2019/04/01 APPLIED Ratchet-1 SVT EC025,EC026,EC027

LCFC 3Pin Symbol rule

Orcad Symbol & PCB Footprint pin assignment

Use common rule, Top side is Pin1, not follow original datasheet definition to avoid confusion with different vender definition. Below is an example.



part supplier pin assignment

LCFC common pin assignment

TABLE: Chip Capacitor Thermal Characteristics

		Code
-55 to 150degC	+/-30ppm/degC	NPO
-55 to 125degC	+/-30ppm/degC	C0G
-55 to 125degC	+/-15%	X7R
-55 to 105degC	+/-22%	X6S
-55 to 85degC	+/-15%	X5R

TABLE: Chip Capacitor Tolerance

Tolerance	Code
+/-0.1pF	B
+/-0.25pF	C
+/-0.5pF	D
+/-5%	J
+/-10%	K
+/-20%	M
+50/-20%	Z

TABLE: Chip Part Dimension

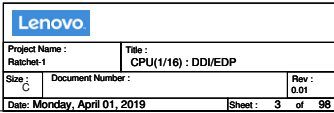
Size [mm]	mm Size Code	Inch Size Code
0.40 x 0.20	0402	01005
0.60 x 0.30	0603	0201
1.00 x 0.50	1005	0402
1.60 x 0.80	1608	0603
2.00 x 1.25	2125	0805
2.00 x 1.60	2016	0806
2.50 x 2.00	2520	1008
3.20 x 1.60	3216	1206
3.20 x 2.50	3225	1210
4.50 x 1.60	4516	1806
4.50 x 2.50	4525	1810
4.50 x 3.20	4532	1812
5.00 x 2.50	5025	2010
6.40 x 3.20	6432	2512

↑
LOGIC

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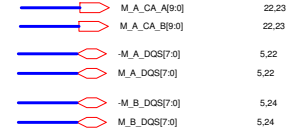
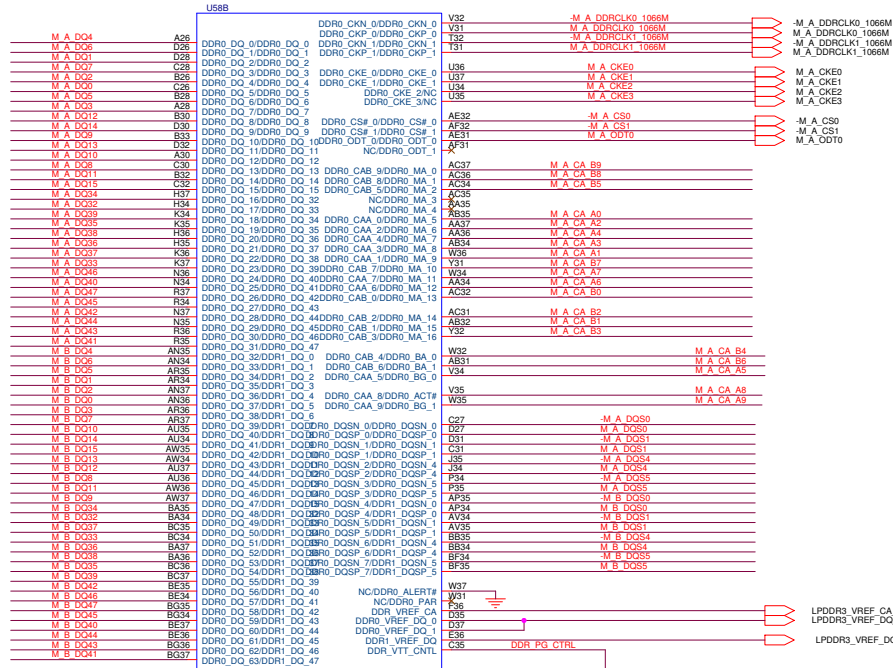
Project Name : Ratchet-1		Title : EC HISTORY	
Size : C	Document Number :	Rev : 0.01	
Date: Monday, April 01, 2019		Sheet : 2	of 98

GPP_E19/DDPB_CTRLDATA(DISPLAY PORT B DETECTED)	
GPP_E21/DDPC_CTRLDATA(DISPLAY PORT C DETECTED)	
GPP_E23/DDPD_CTRLDATA(DISPLAY PORT D DETECTED)	
HIGH	ENABLE
LOW	DISABLE

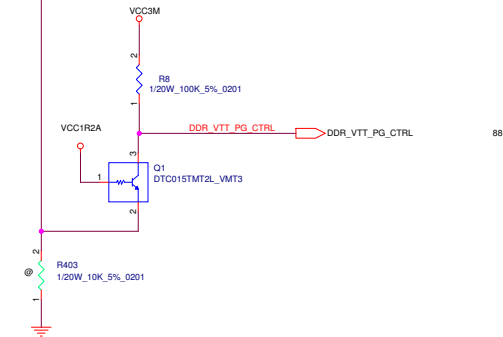


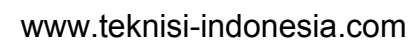
5.22 M_A_DQ[63:0]

5.24 M_B_DQ[63:0]



WHISKEYLAKE-U_BGA1528





SPI0_IO2 (Consent Strap)	
HIGH	Disable (Default)
LOW	Enable

GPP_B23/SML1ALERT#/PCHHOT#	
HIGH	Enable Intel(R) DCI-OOB
LOW	Disable Intel(R) DCI-OOB (Default)

GPP_C2/SMLALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS (Default)

The diagram illustrates the functional strap connections for the WHISKEYLAKE-U_BGA1528 device. It shows the internal connections of the device to various external components, including resistors (R10, R13, R12, R704, R42, R404, R405, R406, R702, R703, R720), capacitors (C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64, C65, C66, C67, C68, C69, C70, C71, C72, C73, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100), and other chips (U1, U2, U3, U4, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, U22, U23, U24, U25, U26, U27, U28, U29, U30, U31, U32, U33, U34, U35, U36, U37, U38, U39, U40, U41, U42, U43, U44, U45, U46, U47, U48, U49, U50, U51, U52, U53, U54, U55, U56, U57, U58, U59, U60, U61, U62, U63, U64, U65, U66, U67, U68, U69, U70, U71, U72, U73, U74, U75, U76, U77, U78, U79, U80, U81, U82, U83, U84, U85, U86, U87, U88, U89, U90, U91, U92, U93, U94, U95, U96, U97, U98, U99, U100). The diagram is divided into several sections, each representing a different functional strap. The connections are color-coded: red for power, blue for ground, green for data, and yellow for control. The diagram is labeled with component values and pin numbers. The title is 'WHISKEYLAKE-U_BGA1528' and the page number is '5 of 20'.

TABLE : Functional Strap

GPP_C5/SML0ALERT# (LPC or eSPI)	
HIGH	eSPI is selected
LOW	LPC is selected (Default)

← LOGIC

TABLE : Functional Strap

GPP_B18/GSPI0_MOSI (No Reboot)	
HIGH	Enable "No Reboot" Mode
LOW	Disable "No Reboot" Mode (Default)

← LOGIC

TABLE : Functional Strap

GPP_B22/GSPI1_MOSI (Boot BIOS Destination)	
HIGH	Boot BIOS from LPC
LOW	Boot BIOS from SPI(Default)

← LOGIC

TABLE : Functional Strap

GPP_F6/CNV_RGI_DT(M.2 CNVI Mode Select)	
HIGH	Integrated CNVI Disabled
LOW	Integrated CNVI Enabled

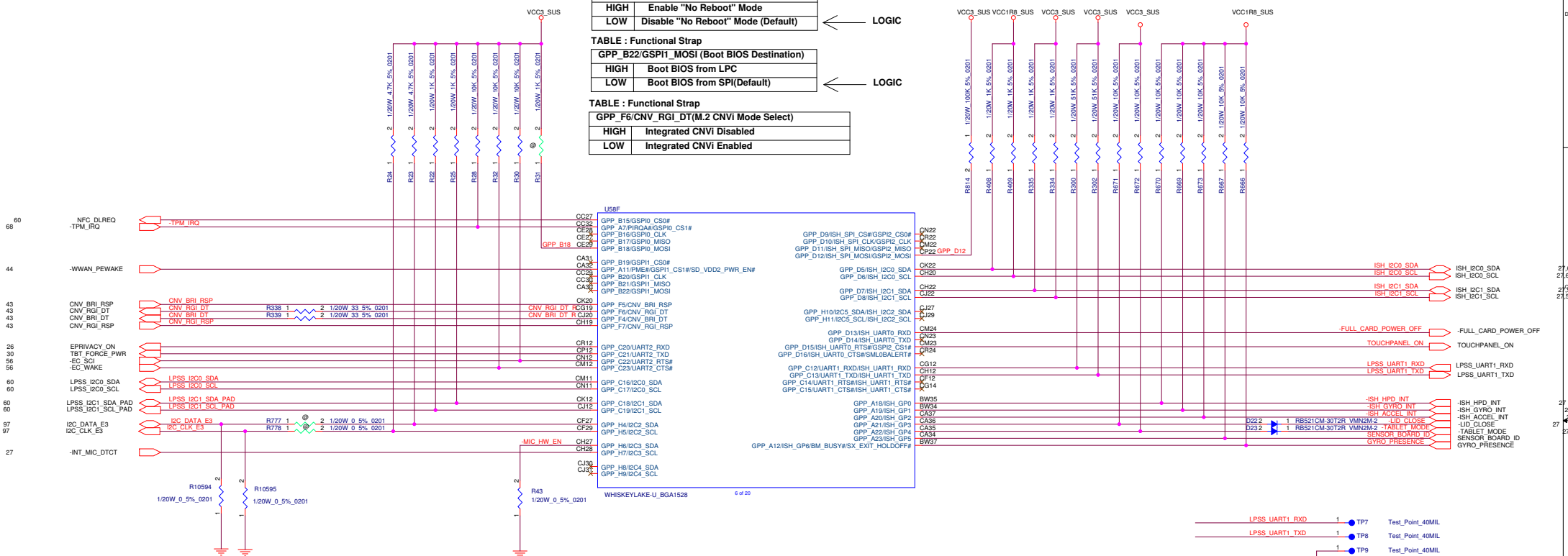


TABLE : Functional Strap

GPP_D12(JTAG ODT Disable)	
HIGH	JTAG ODT Enable (Default)
LOW	JTAG ODT Disable

← LOGIC

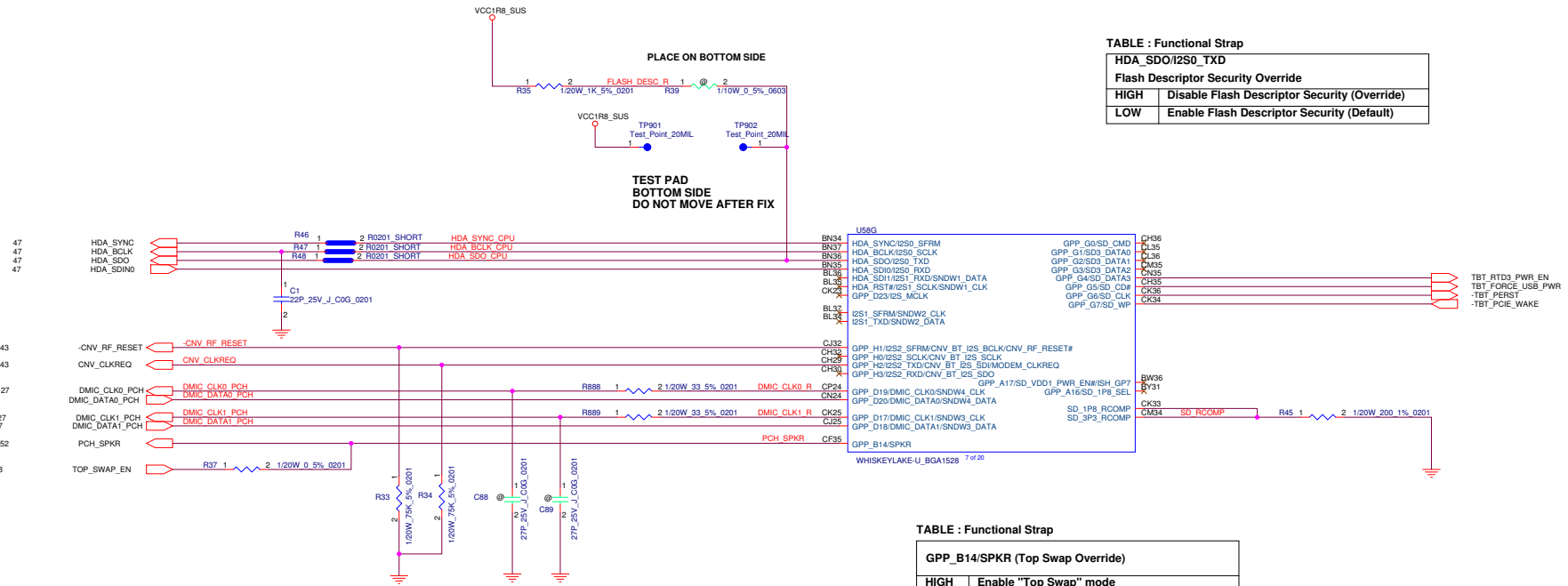


TABLE : Functional Strap

HDA_SDO/I2S0_TXD	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

TABLE : Functional Strap

GPP_B14/SPKR (Top Swap Override)	
HIGH	Enable "Top Swap" mode
LOW	Disable "Top Swap" mode (Default)

← LOGIC

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GPP_H23(eSPI Flash Sharing Mode)	
HIGH	Enable SAFS
LOW	Enable MAFS(Default)

GPP_H21 (XTAL Frequency Select)	
HIGH	24MHz XTAL selected
LOW	38.4MHz XTAL frequency selected (Default)

[illegible]

MEMORYID[4:0]	U170,U171,U172,U173			Capacity
00h (00000b)	Samsung	K4E6E304EC-EGCG	16Gbit DDP	8GB
01h (00001b)		K4EBE304EC-EGCG	32Gbit QDP	16GB
02h (00010b)	SK hynix	H9CCNNNB7J1ALR-NVD	16Gbit DDP	8GB
03h (00011b)		H9CCNNNCLGALAR-NVD	32Gbit QDP	16GB
04h (00100b)	Samsung	K4E6E304EB-EGCG	16Gbit DDP	8GB
05h (00101b)		K4EBE304EB-EGCG	32Gbit QDP	16GB
06h (00110b)		K4E6E304ED-EGCG	16Gbit DDP	8GB
07h (00111b)		K4EBE304ED-EGCG	32Gbit QDP	16GB
08h (01000b)	Nanya	NT6CL512T32AM-H0	16Gbit DDP	8GB

LEVEL	PLANAR ID			
	3	2	1	0
	R1102	R1103	R1104	R1105
1	NA	NA	NA	NA
0	ASM	ASM	ASM	ASM

LEVEL	PLANARID[3:0]
EVT	0000B
FVT	0001B
ME SIT	0010B
SIT	0011B
SVT	0100B

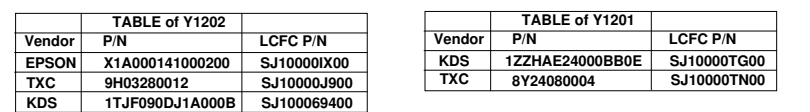
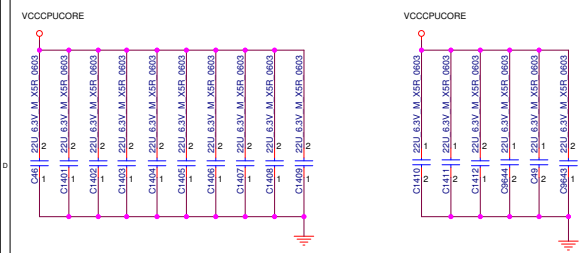


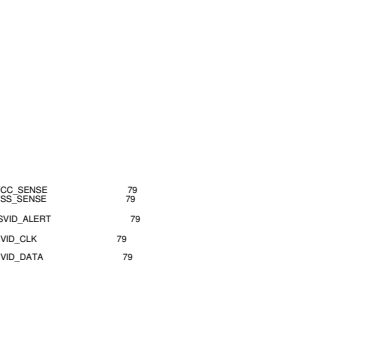
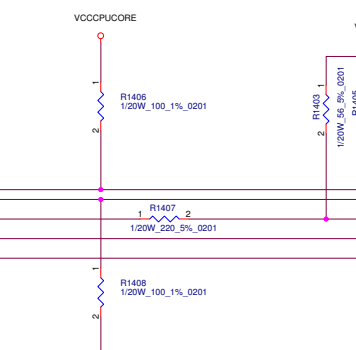
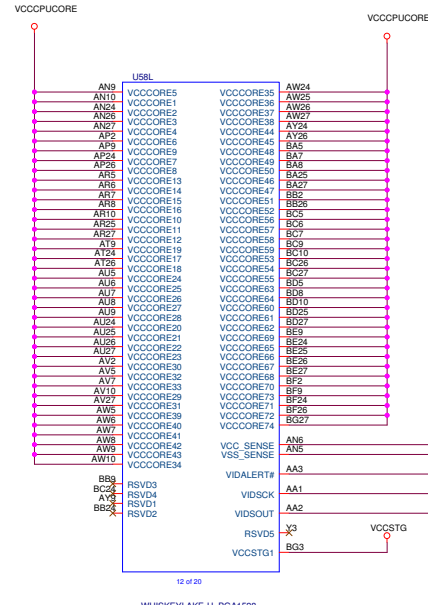
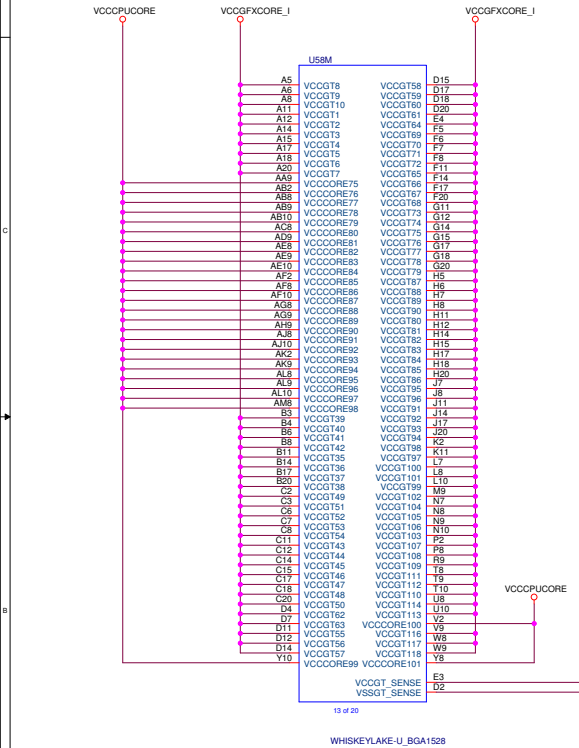
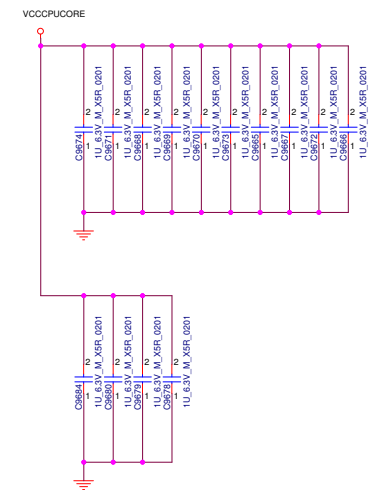
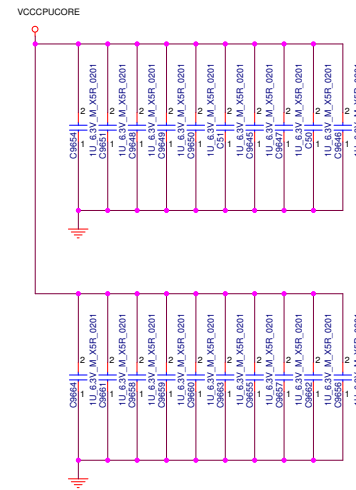
	TABLE of Y1202	
Vendor	P/N	LCFC P/N
EPSON	X1A000141000200	SJ10000IX00
TXC	9H03280012	SJ10000J900
KDS	1TJF090DJ1A000B	SJ100069400

	TABLE of Y1201	
Vendor	P/N	LCFC P/N
KDS	1ZZHAE24000BB0E	SJ10000TG00
TXC	8Y24080004	SJ10000TN00

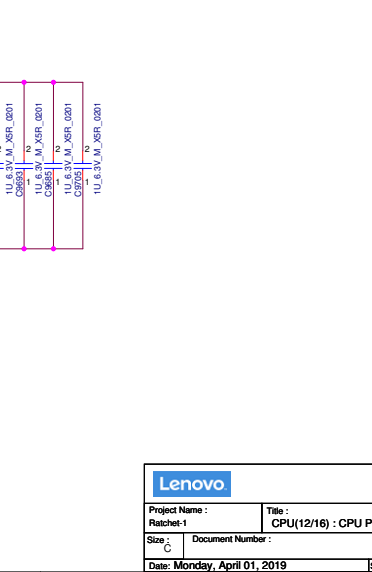
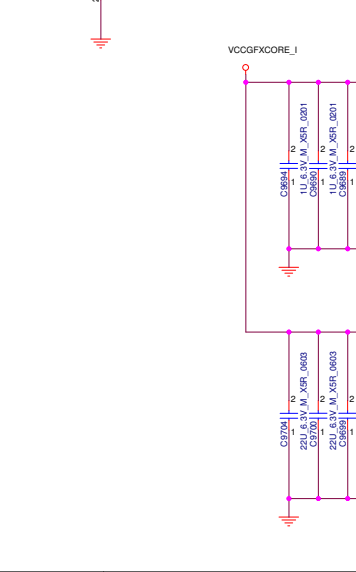
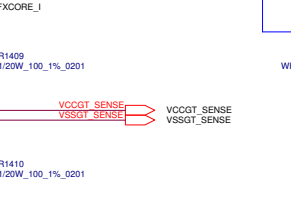
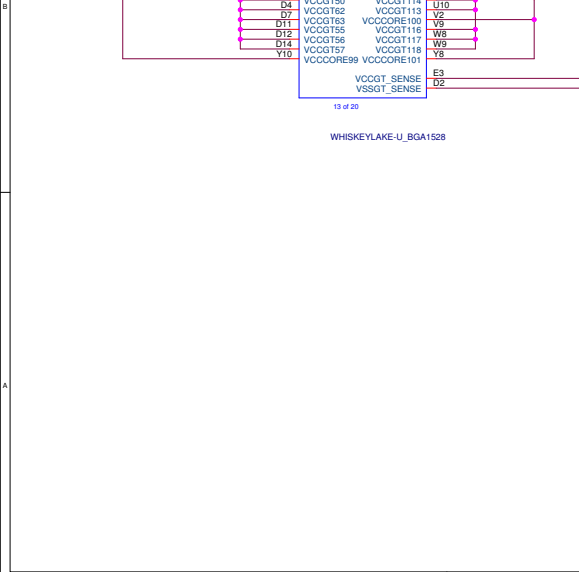


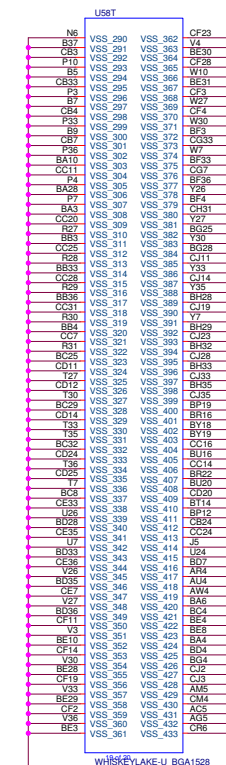
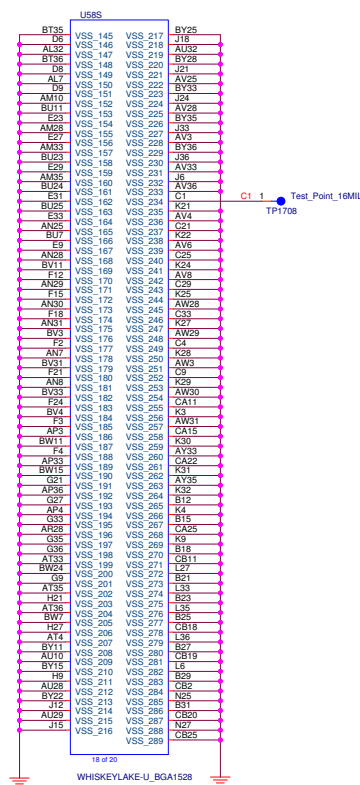
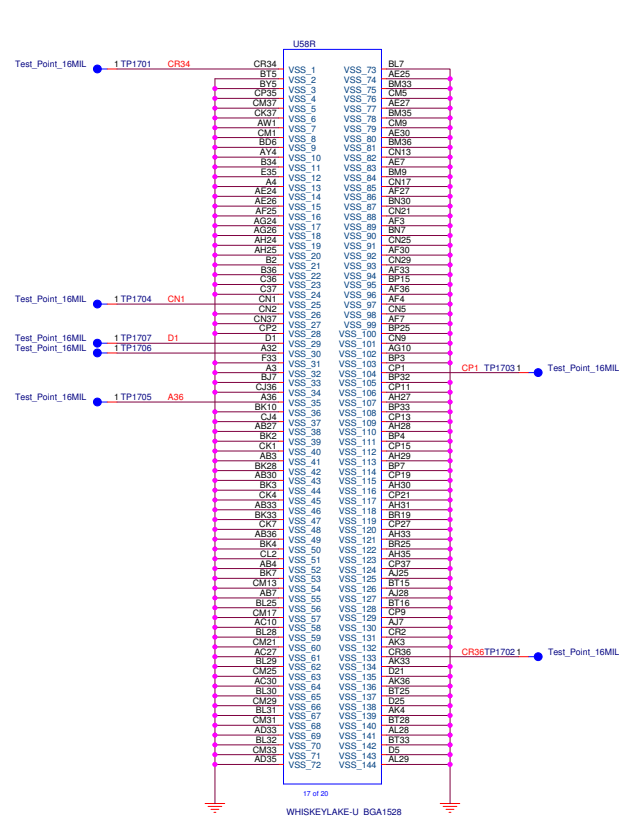
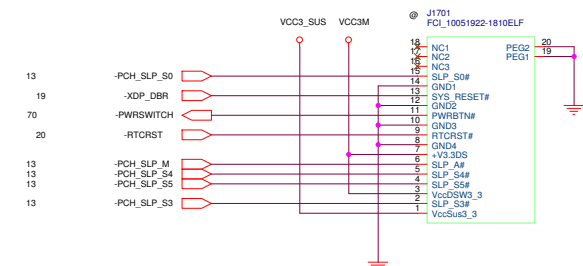
VccGT	PDG	Ratchet
330uF	0	HW: 0/PWR: 1
220uF	2	HW: 0/PWR: 0
47uF	4	HW: 0/PWR: 0
22uF	15	HW: 7/PWR: 25
10uF	15	HW: 0/PWR: 0
1uF	11	HW: 11/PWR: 0

VccCORE	PDG	Ratchet
330uF	0	HW: 0/PWR: 2
220uF	4	HW: 0/PWR: 0
47uF	18	HW: 0/PWR: 0
22uF	9	HW: 16/PWR: 25
10uF	22	HW: 0/PWR: 0
1uF	42	HW: 34/PWR: 0



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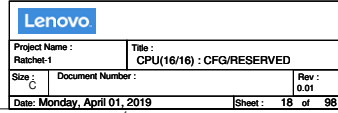


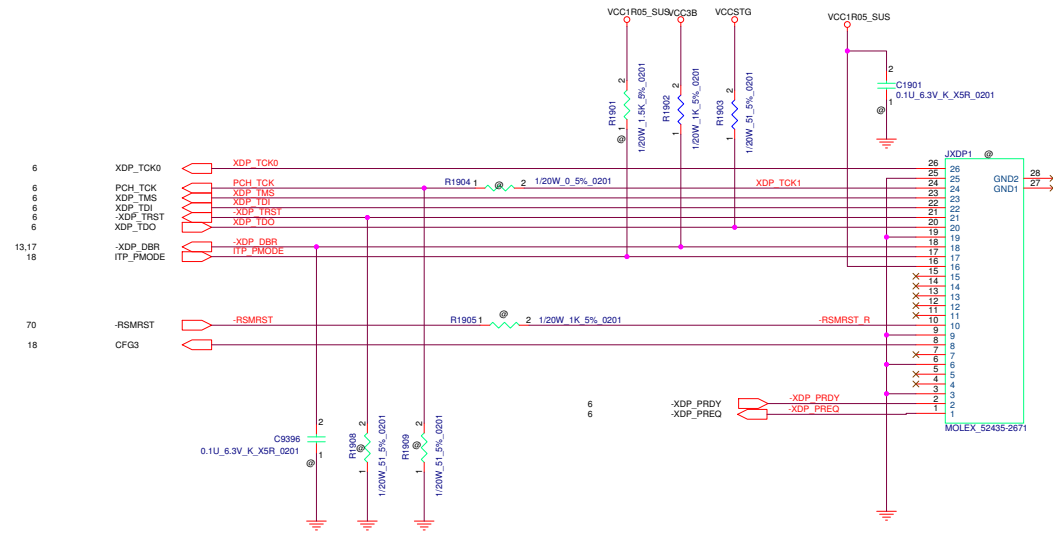
CFG0: Stall Reset Sequence after PCU PLL Lock untill de-asserted 1:No Stall 0: Stall
CFG3: MSR Privacy Bit Feature 1: MSR (C80h) bit[0] setting 0: MSR (C80h) bit[0] overridden
CFG4: eDP Enable 1:Disabled 0:Enabled
CFG9: SVID Bus Communication 1:Enabled 0:Disabled

U580		
K12	RSVD048	
K13	RSVD047	RSVD38
K14	RSVD049	RSVD39
K15	RSVD040	RSVD40
K16	RSVD050	RSVD41
K17	RSVD51	RSVD42
K18	RSVD042	RSVD43
L1	RSVD53	RSVD44
M1	RSVD54	RSVD45
M2	RSVD55	
P1	RSVD56	RSVD64
P2	RSVD57	RSVD65
R1	RSVD58	
R2	RSVD59	
W25	RSVD60	
Y25	RSVD61	
Y26	RSVD62	
Y27	RSVD63	

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WHISKEYLAKE-U_BGA1528

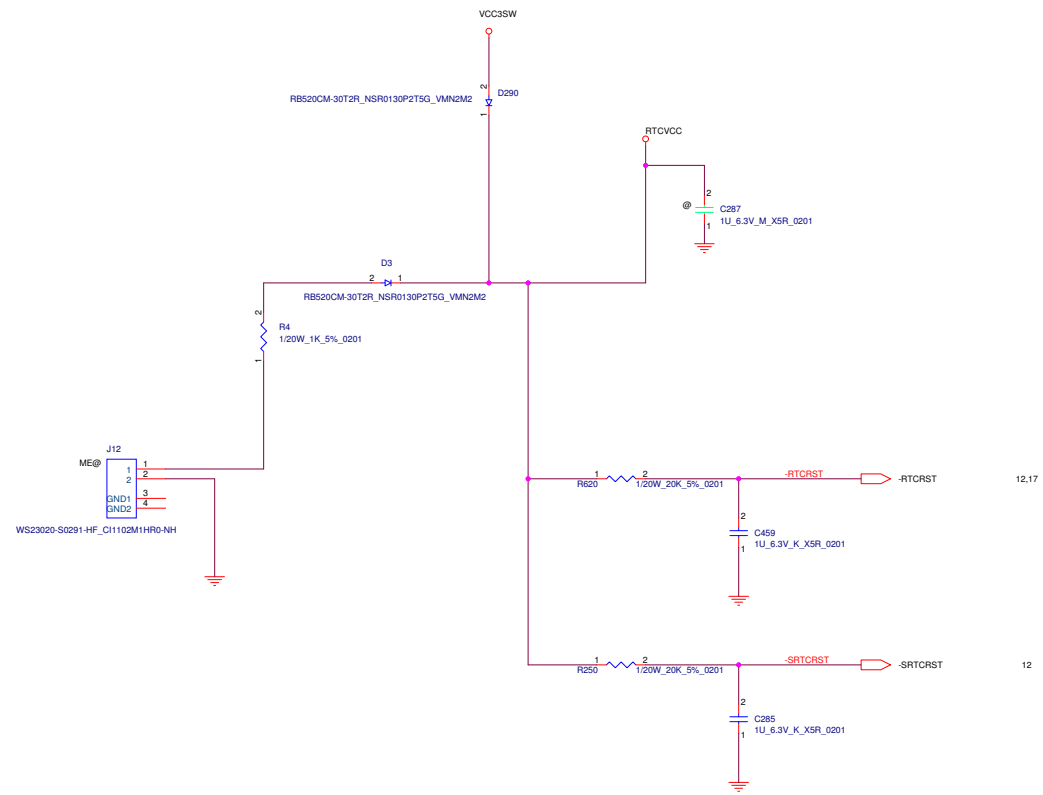




TABLE

Logic	Ref Des	Merged	DCI 2.0
Page 6	R10607	ASM	NO_ASM
	R10608	ASM	NO_ASM
Page 7	R42	ASM	NO_ASM
Page 18	R1801	ASM	NO_ASM
Page 19	JXDP1	ASM	NO_ASM
	C1901	ASM	NO_ASM
	R1903	ASM	ASM
	R1902	ASM	ASM
	R1901	ASM	NO_ASM
	R1905	ASM	NO_ASM
	R1904	ASM	NO_ASM

↑
LOGIC



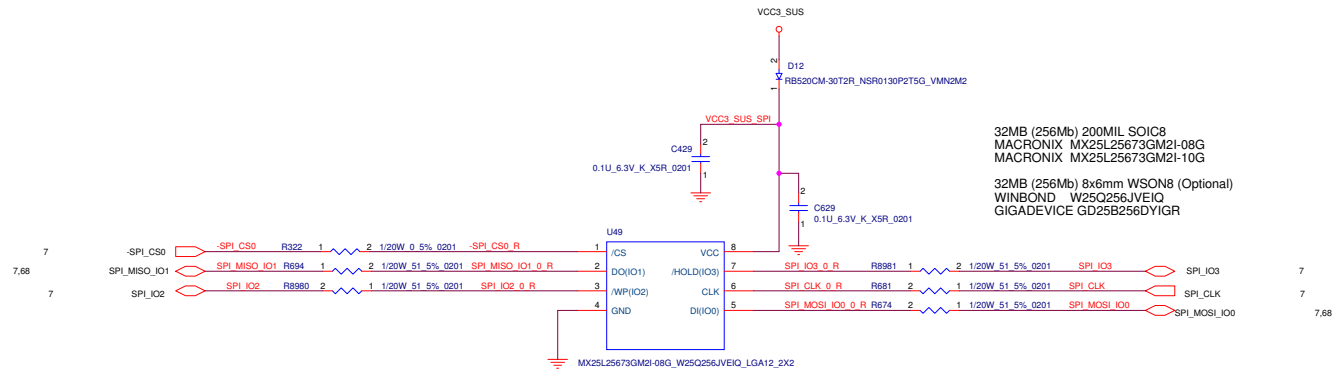
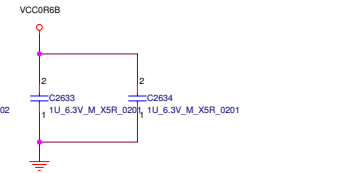
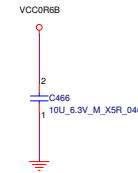
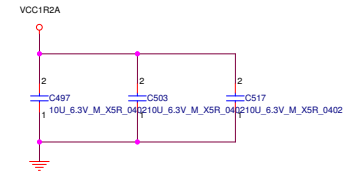
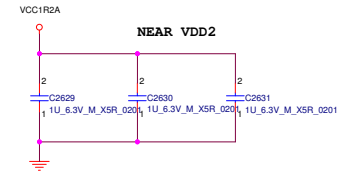
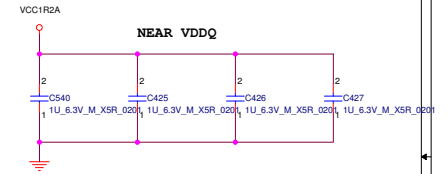
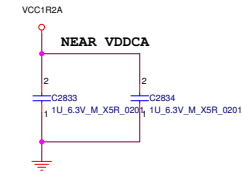
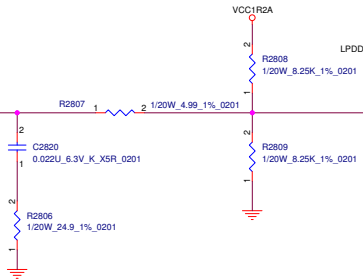
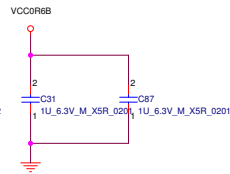
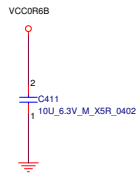
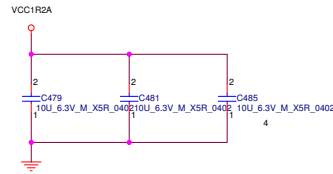
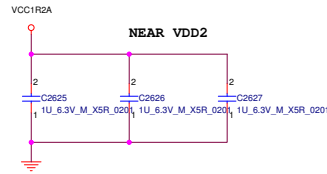
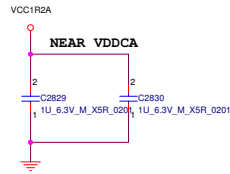
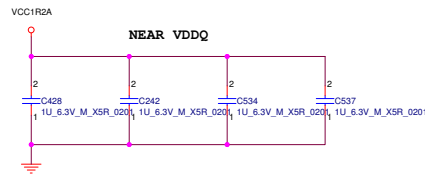
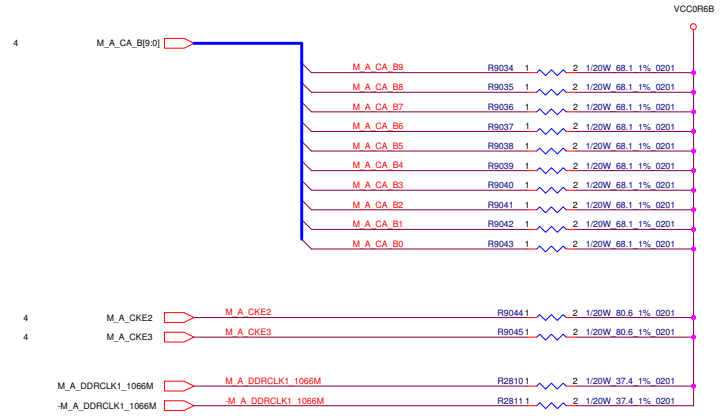
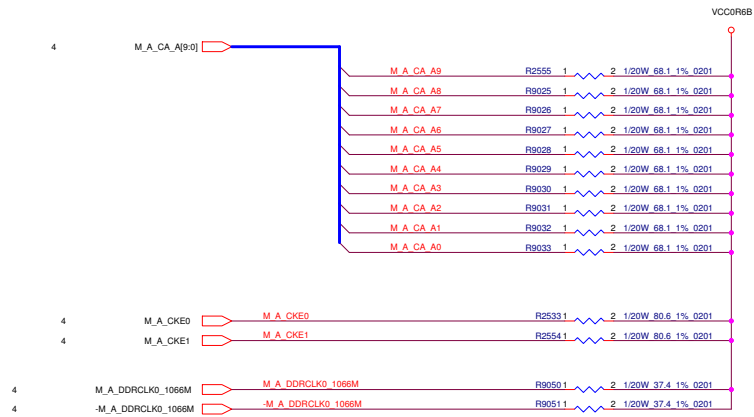
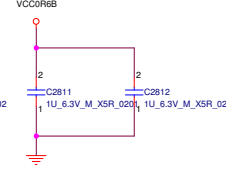
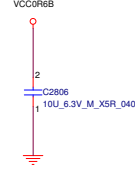
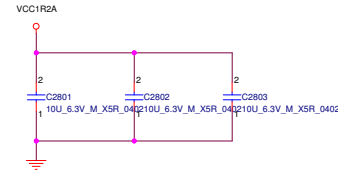
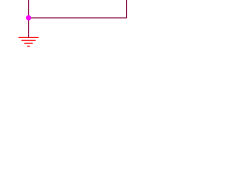
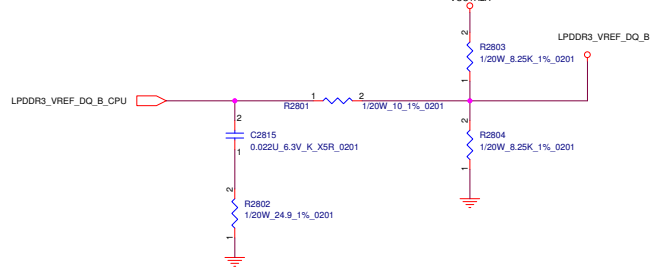
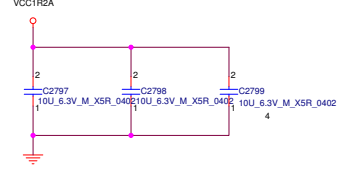
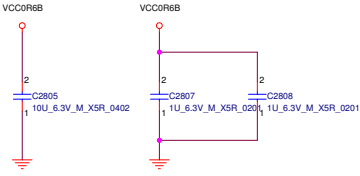
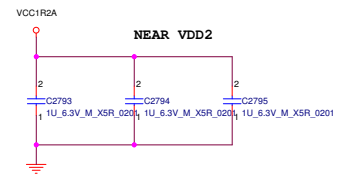
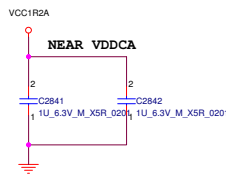
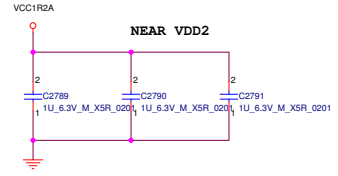
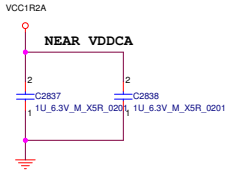
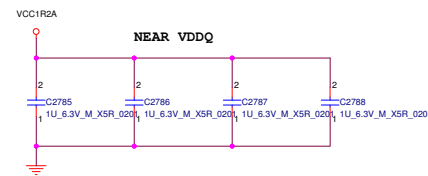
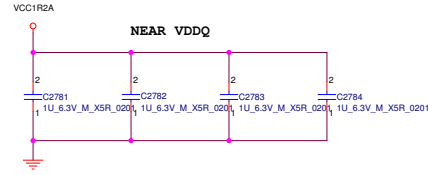
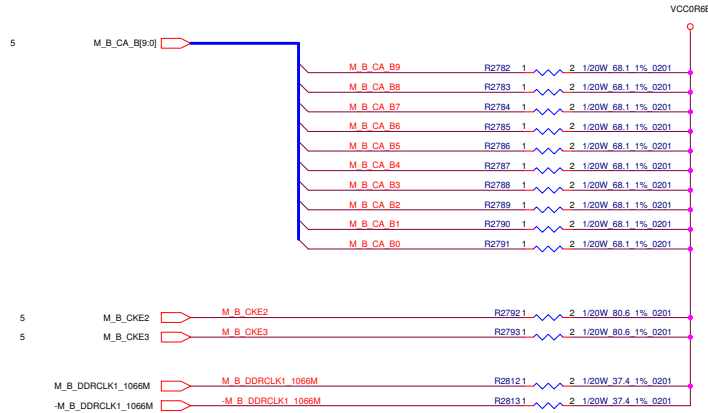
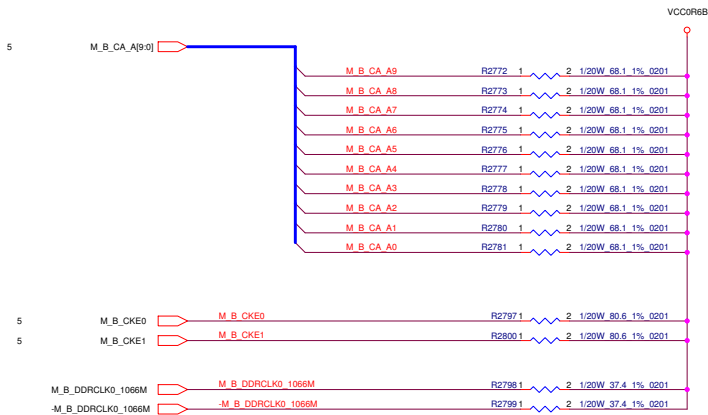


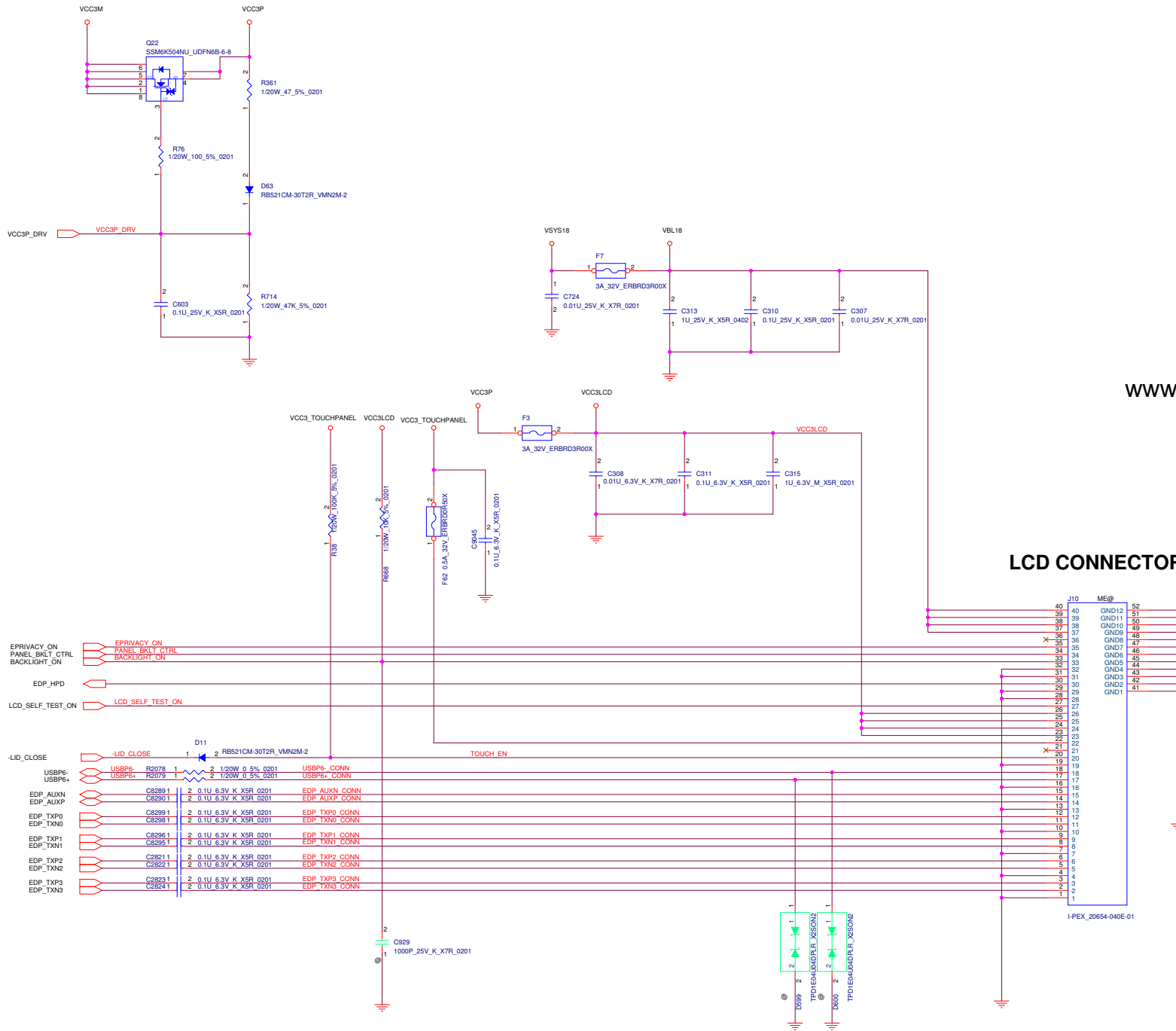
TABLE							
SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	GND	2		
3	CS#	R322.2	R681.2	CLK	4		
5	MISO	R694.2	R674.2	MOSI	6		
7	(KEY)	N/A	N/A	(RESET)	8		



Supplier	Capacity	Supplier's P/N	Package Size		Die	Configuration	ZQ0/ZQ	ZQ1/NC	Dual Ch
Samsung	16Gb	K4E6E304EB-EGCG	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
		K4E6E304ED-EGCG	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
	32Gb	K4EBE304EB-EGCG	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
		K4EBE304ED-EGCG	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
SK hynix	16Gb	H9CCNNNBJTLAR-NVD	11.0 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB
	32Gb	H9CCNNNCLGALAR-NVD	11.0 x 11.5 mm	QDP	8Gb (512M x16)	2 Rank x (512M x32)	ZQ0	ZQ1	16GB
Nanya	16Gb	NT6CL512T32AM-H0	10.5 x 11.5 mm	DDP	8Gb (256M x32)	2 Rank x (256M x32)	ZQ	NC	8GB

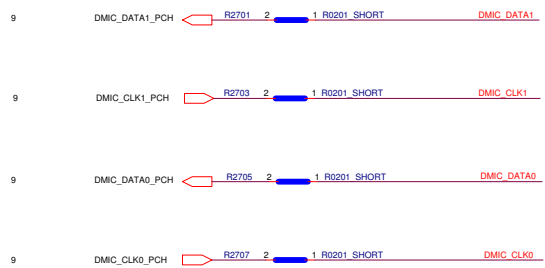






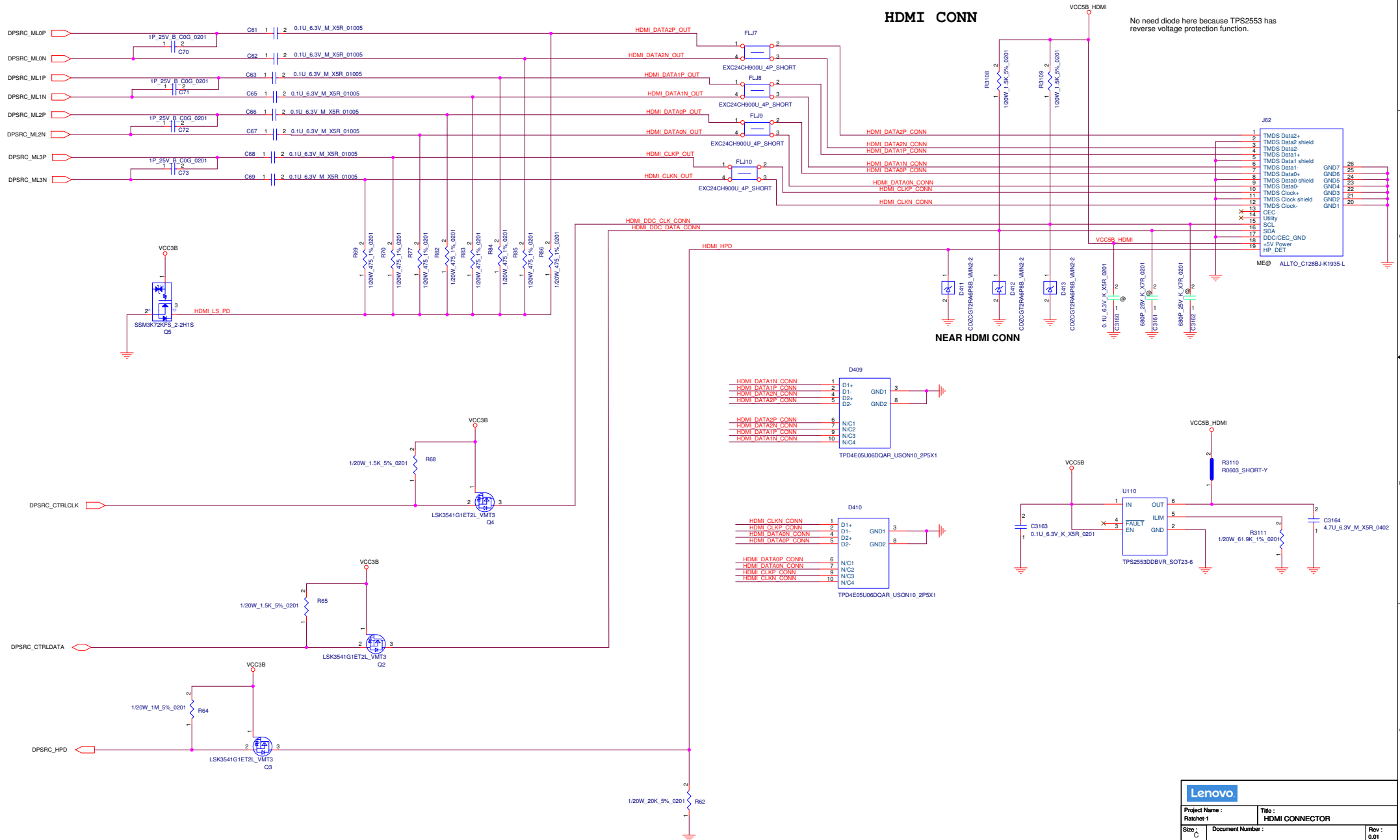
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LCD CONNECTOR

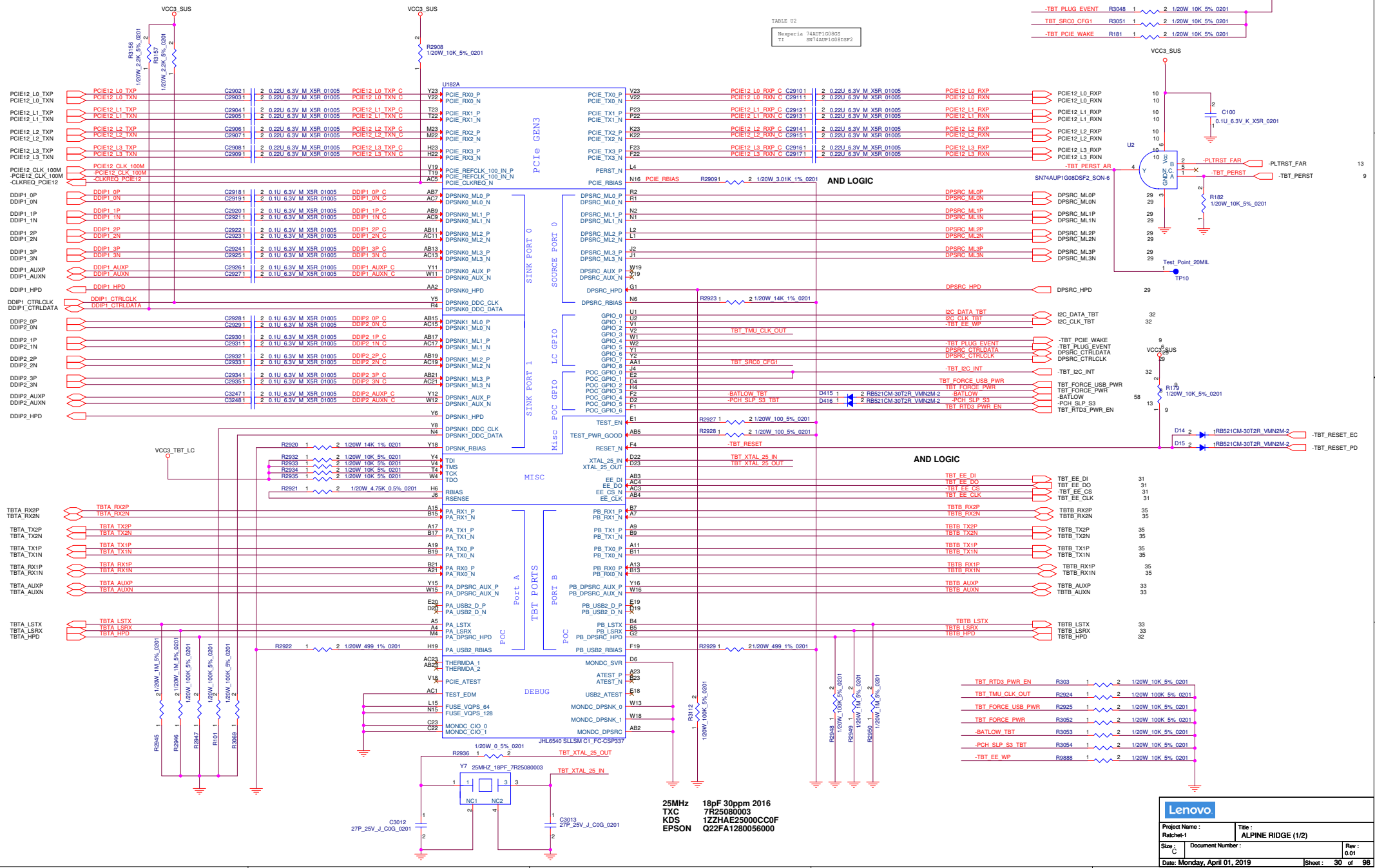


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Size : C	Document Number :	Rev : 0.01
Date: Monday, April 01, 2019		Sheet : 28 of 98

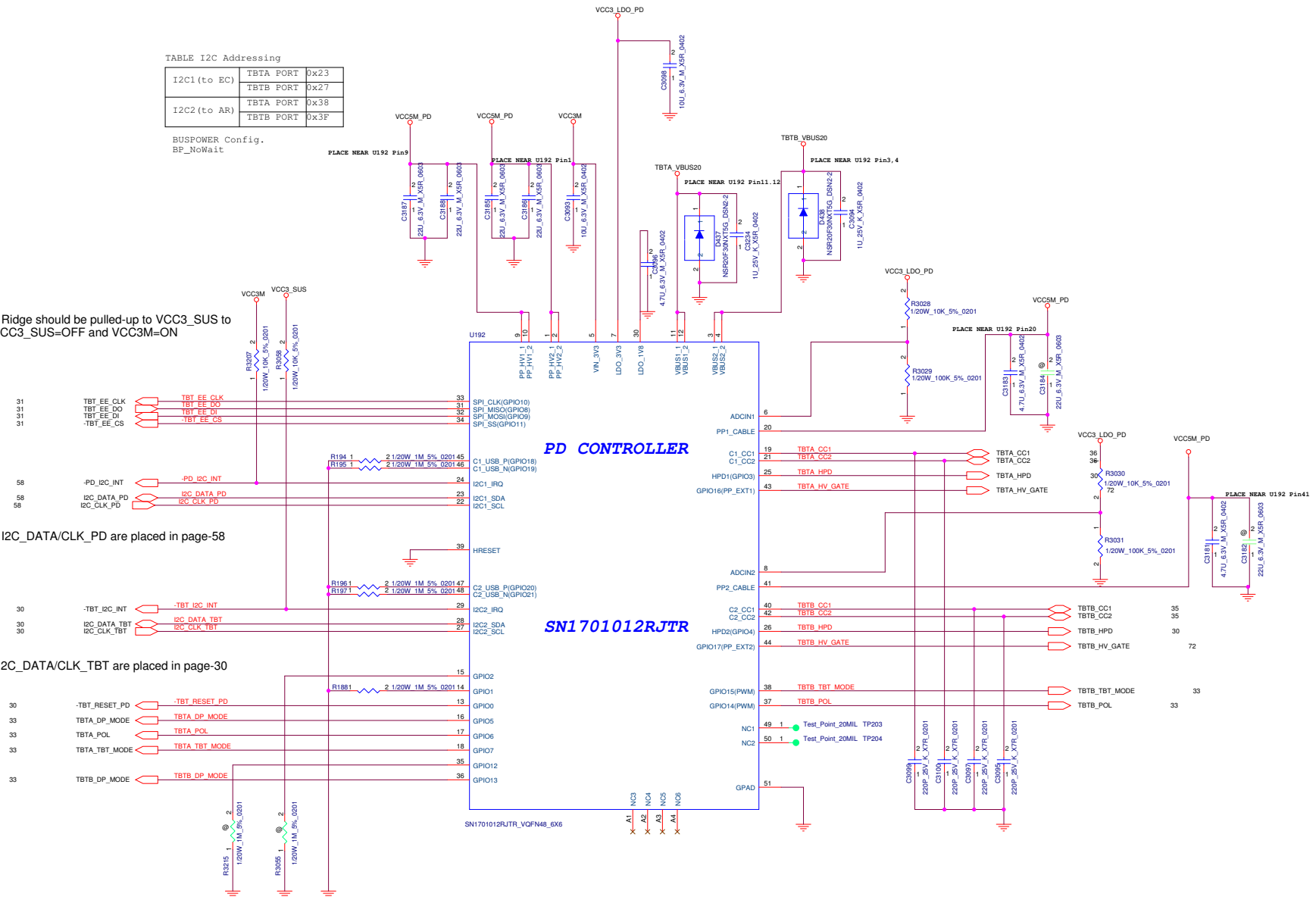


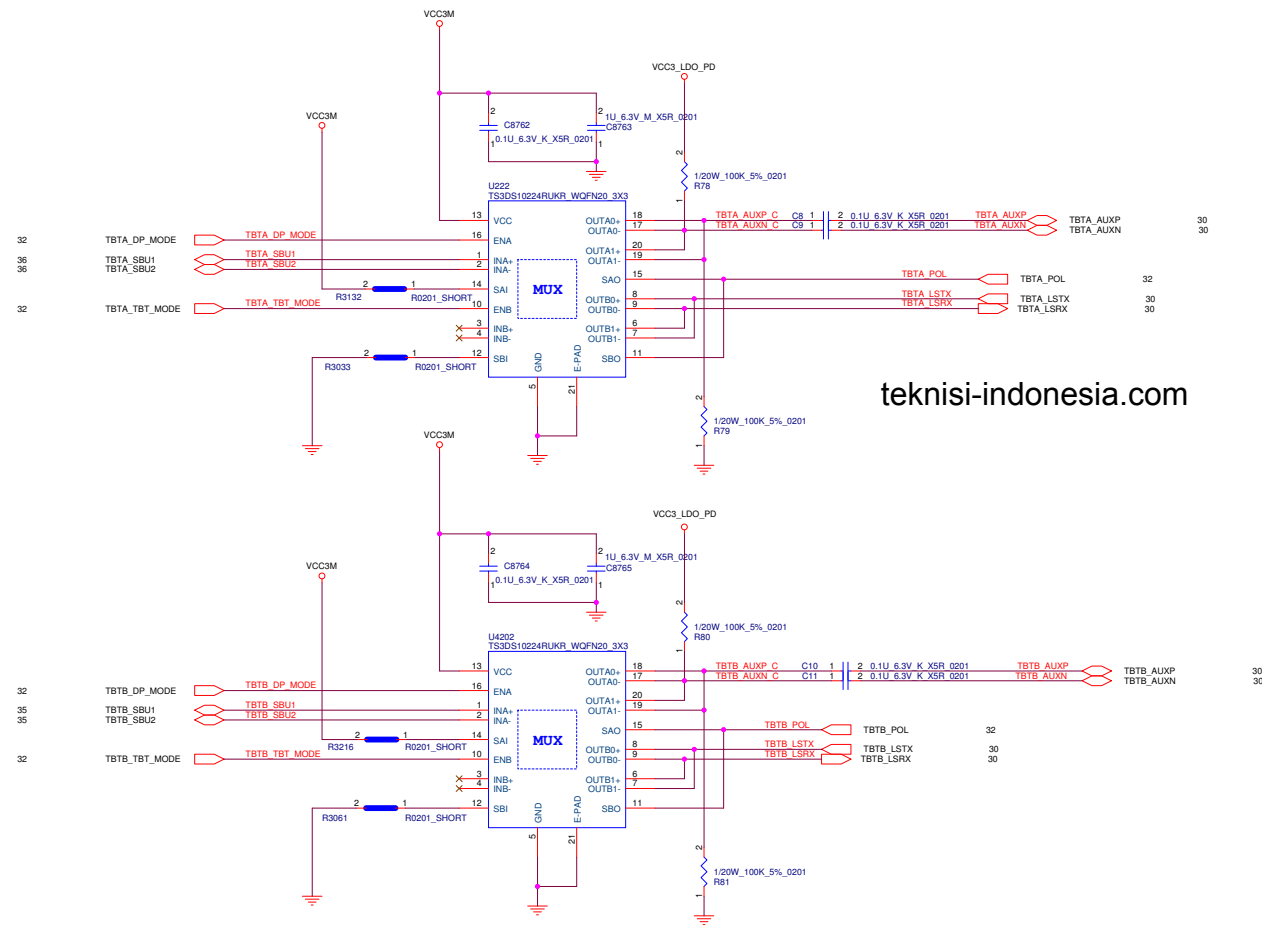
I2C from PD for Alpine Ridge should be pulled-up to VCC3_SUS to prevent leakage when VCC3_SUS=OFF and VCC3M=ON



I2C1 (to EC)	TBTA PORT	0x23
	TBTB PORT	0x27
I2C2 (to AR)	TBTA PORT	0x38
	TBTB PORT	0x3F

GPI02/12 can be floating when unused.

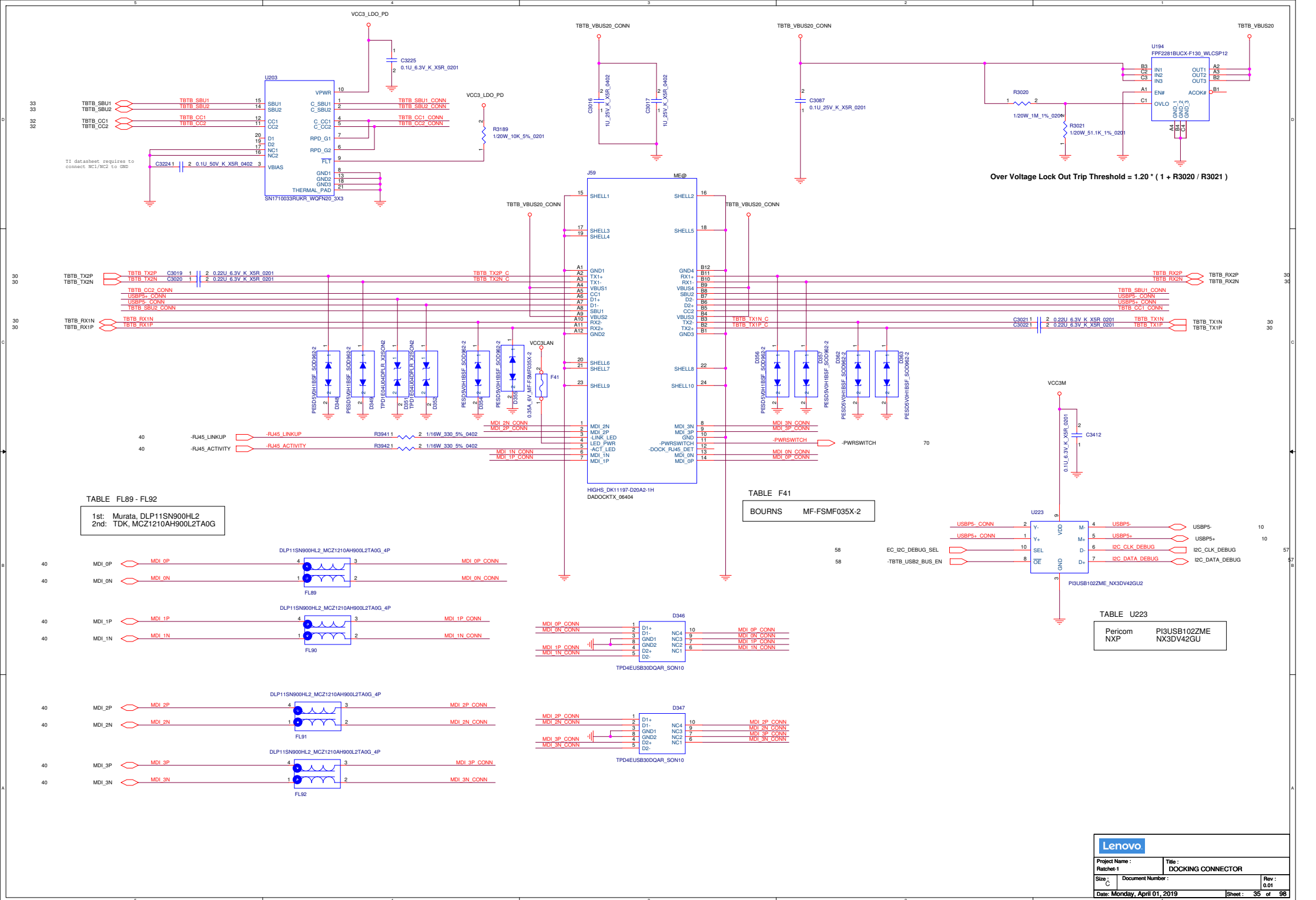


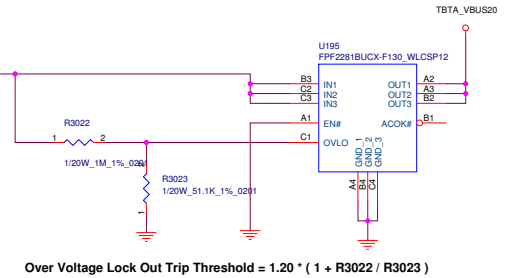
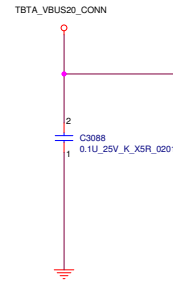
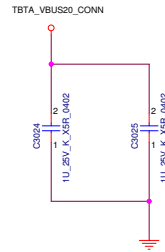
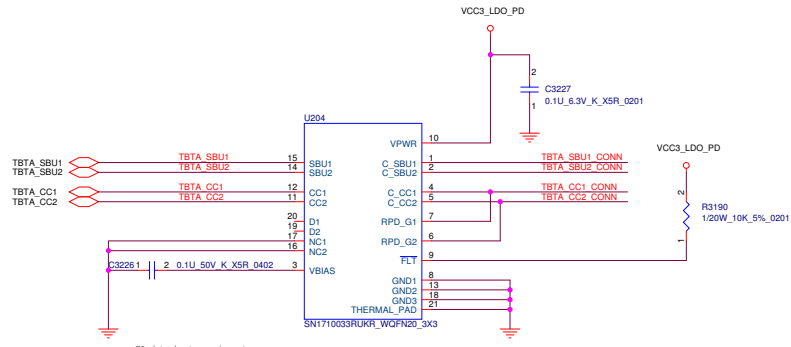


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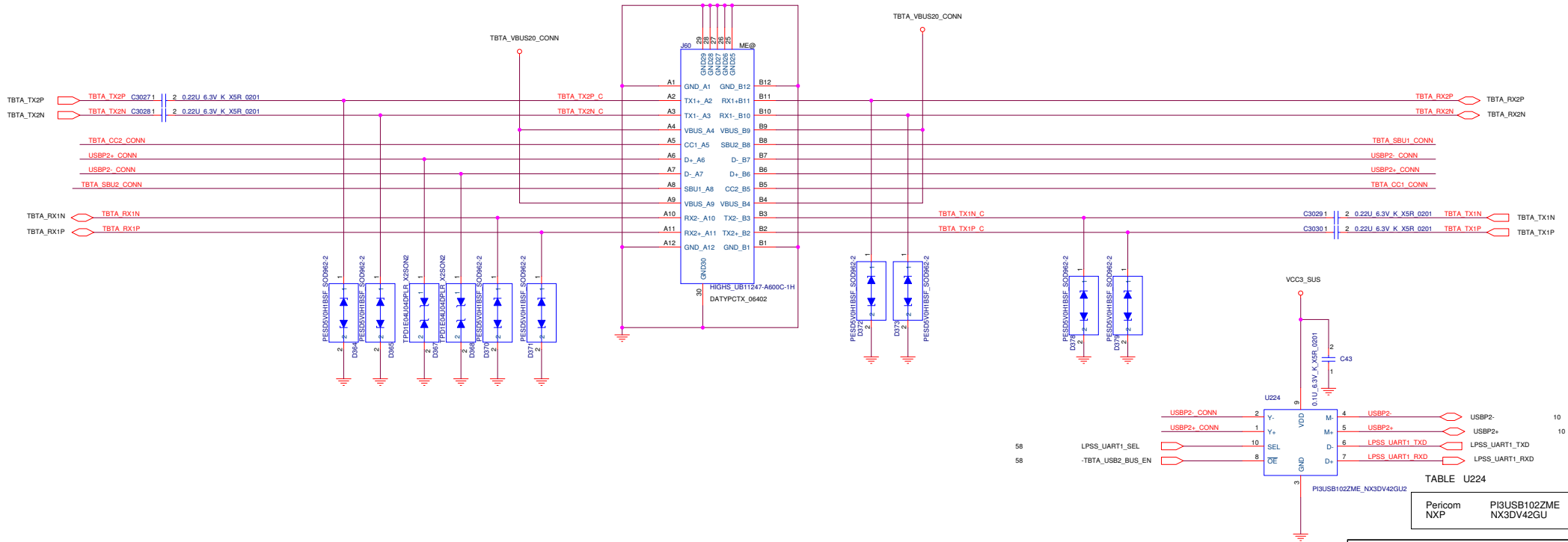
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Date: Monday, April 01, 2019		Sheet : 34 of 98

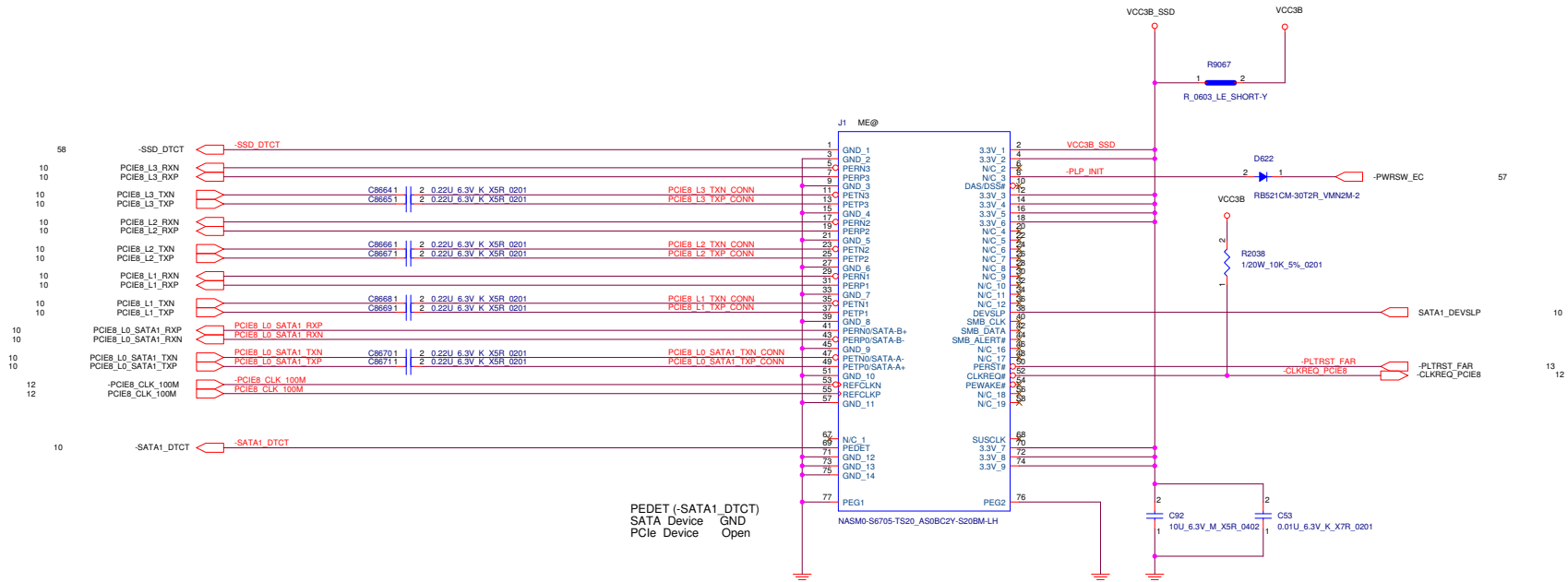




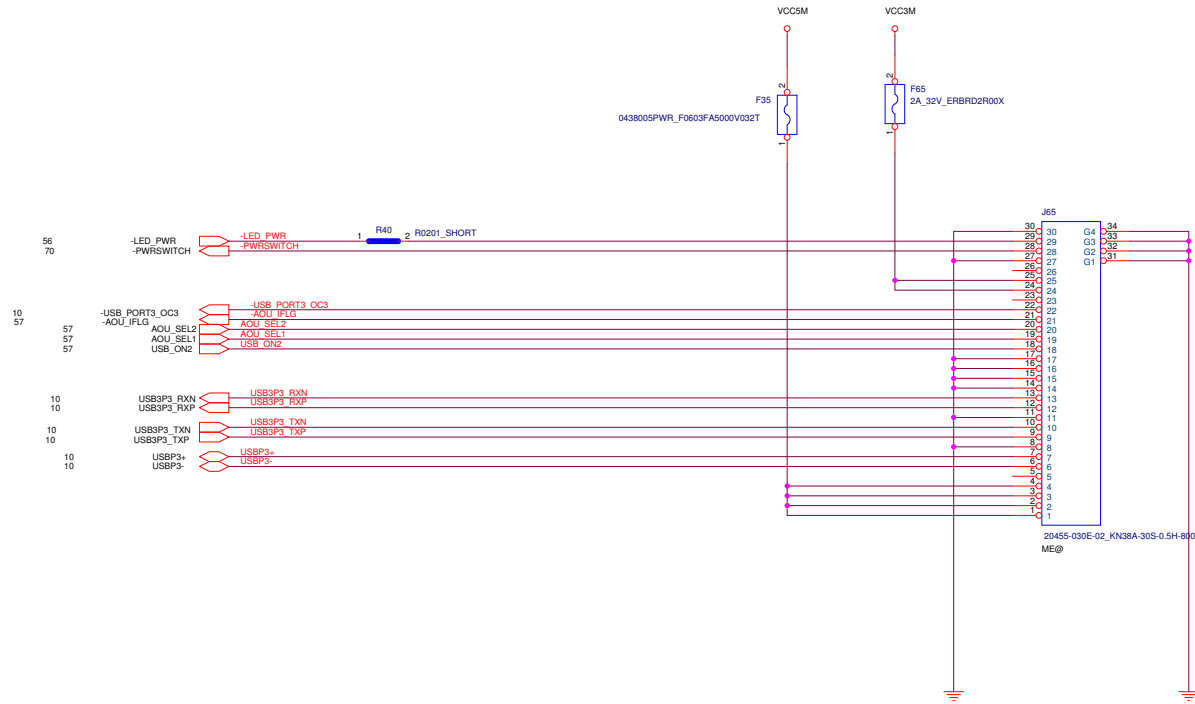
Over Voltage Lock Out Trip Threshold = $1.20 * (1 + R3022 / R3023)$



M.2 Socket 3 (Key-M) for 2280 S3 SSD
H=2.00mm Connector




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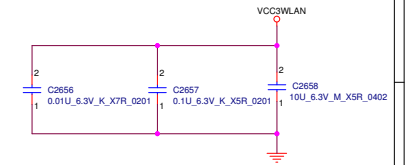
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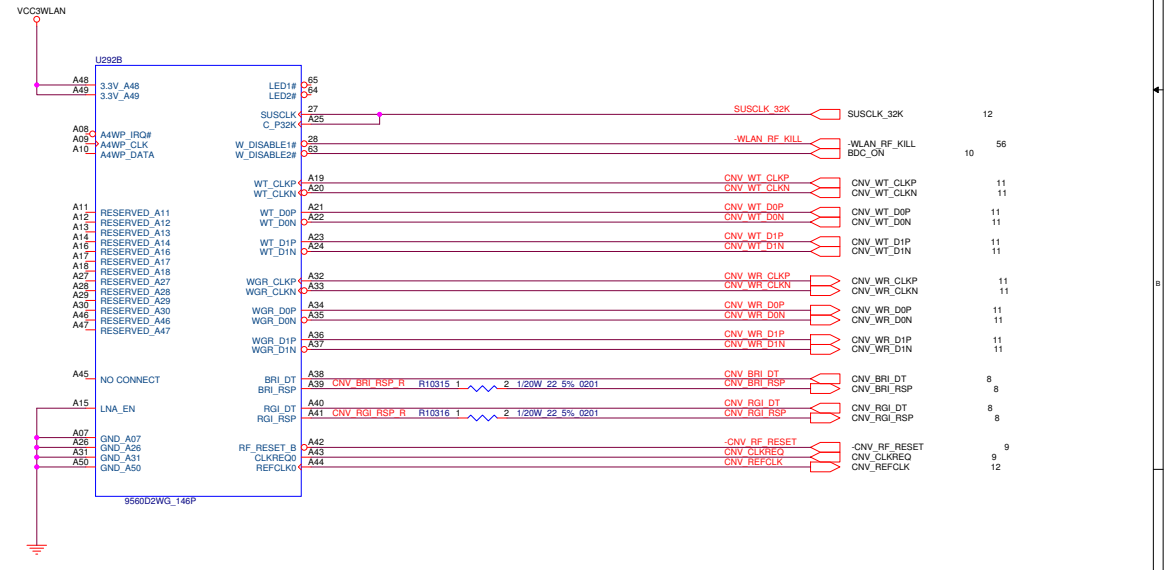
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Size : C	Document Number :	Rev : 0.01
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U292A

Pin	Function	Pin	Function
1	UIM_POWER_SRC/GPIO1	25	RESERVED_16
2	UIM_PWR_SNK	26	RESERVED_17
3	UIM_SWP	27	RESERVED_18
4	3.3V_4	28	RESERVED_19
5	3.3V_5	29	RESERVED_20
6	3.3V_6	30	RESERVED_21
7	3.3V_7	31	RESERVED_22
8	ALERT#	32	RESERVED_23
9	I2C_CLK	33	RESERVED_24
10	I2C_DATA	34	RESERVED_25
11	COEX_TXD	35	RESERVED_26
12	COEX_RXD	36	RESERVED_27
13	COEX_SWP	37	RESERVED_28
14	COEX_TXD	38	RESERVED_29
15	COEX_RXD	39	RESERVED_30
16	COEX_SWP	40	RESERVED_31
17	USB_D-	41	RESERVED_32
18	USB_D+	42	RESERVED_33
19	REFCLK0N	43	RESERVED_34
20	REFCLK0P	44	RESERVED_35
21	CLKREQ#	45	RESERVED_36
22	PERNO	46	RESERVED_37
23	PERPO	47	RESERVED_38
24	PETNO	48	RESERVED_39
25	PETPO	49	RESERVED_40
26	PERST#	50	RESERVED_41
27	PEWAKE#	51	RESERVED_42
28	SYSLINK0SNS0	52	RESERVED_43
29	TX_ILANKING0SNS1	53	RESERVED_44
30	SDIO_CLK	54	RESERVED_45
31	SDIO_CMD	55	RESERVED_46
32	SDIO_DATA0	56	RESERVED_47
33	SDIO_DATA1	57	RESERVED_48
34	SDIO_DATA2	58	RESERVED_49
35	SDIO_DATA3	59	RESERVED_50
36	SDIO_RESET#	60	RESERVED_51
37	SDIO_WAKE#	61	RESERVED_52
38	PCM_SYNC02S_WS	62	RESERVED_53
39	PCM_CLKI2S_GLK	63	RESERVED_54
40	PCM_OUTI2S_SD_OUT	64	RESERVED_55
41	PCM_INI2S_SD_IN	65	RESERVED_56
42	LPSS_UART_RXDIBRI_RSP	66	RESERVED_57
43	LPSS_UART_TXDRGI_DT	67	RESERVED_58
44	LPSS_UART_RTSIBRI_DT	68	RESERVED_59
45	LPSS_UART_CTSRGI_RSP	69	RESERVED_60
46	UART_WAKE#	70	RESERVED_61
47		71	RESERVED_62
48		72	RESERVED_63
		73	RESERVED_64
		74	RESERVED_65
		75	RESERVED_66
		76	RESERVED_67
		77	RESERVED_68
		78	RESERVED_69
		79	RESERVED_70
		80	RESERVED_71
		81	RESERVED_72
		82	RESERVED_73
		83	RESERVED_74
		84	RESERVED_75
		85	RESERVED_76
		86	RESERVED_77
		87	RESERVED_78
		88	RESERVED_79
		89	RESERVED_80
		90	RESERVED_81
		91	RESERVED_82
		92	RESERVED_83
		93	RESERVED_84
		94	RESERVED_85
		95	RESERVED_86
		96	RESERVED_87
		97	RESERVED_88
		98	RESERVED_89
		99	RESERVED_90
		100	RESERVED_91
		101	RESERVED_92
		102	RESERVED_93
		103	RESERVED_94
		104	RESERVED_95
		105	RESERVED_96
		106	RESERVED_97
		107	RESERVED_98
		108	RESERVED_99
		109	RESERVED_100
		110	RESERVED_101
		111	RESERVED_102
		112	RESERVED_103
		113	RESERVED_104
		114	RESERVED_105
		115	RESERVED_106
		116	RESERVED_107
		117	RESERVED_108
		118	RESERVED_109
		119	RESERVED_110
		120	RESERVED_111
		121	RESERVED_112
		122	RESERVED_113
		123	RESERVED_114
		124	RESERVED_115
		125	RESERVED_116
		126	RESERVED_117
		127	RESERVED_118
		128	RESERVED_119
		129	RESERVED_120
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		131	RESERVED_122
		132	RESERVED_123
		133	RESERVED_124



H=2.00mm Connector



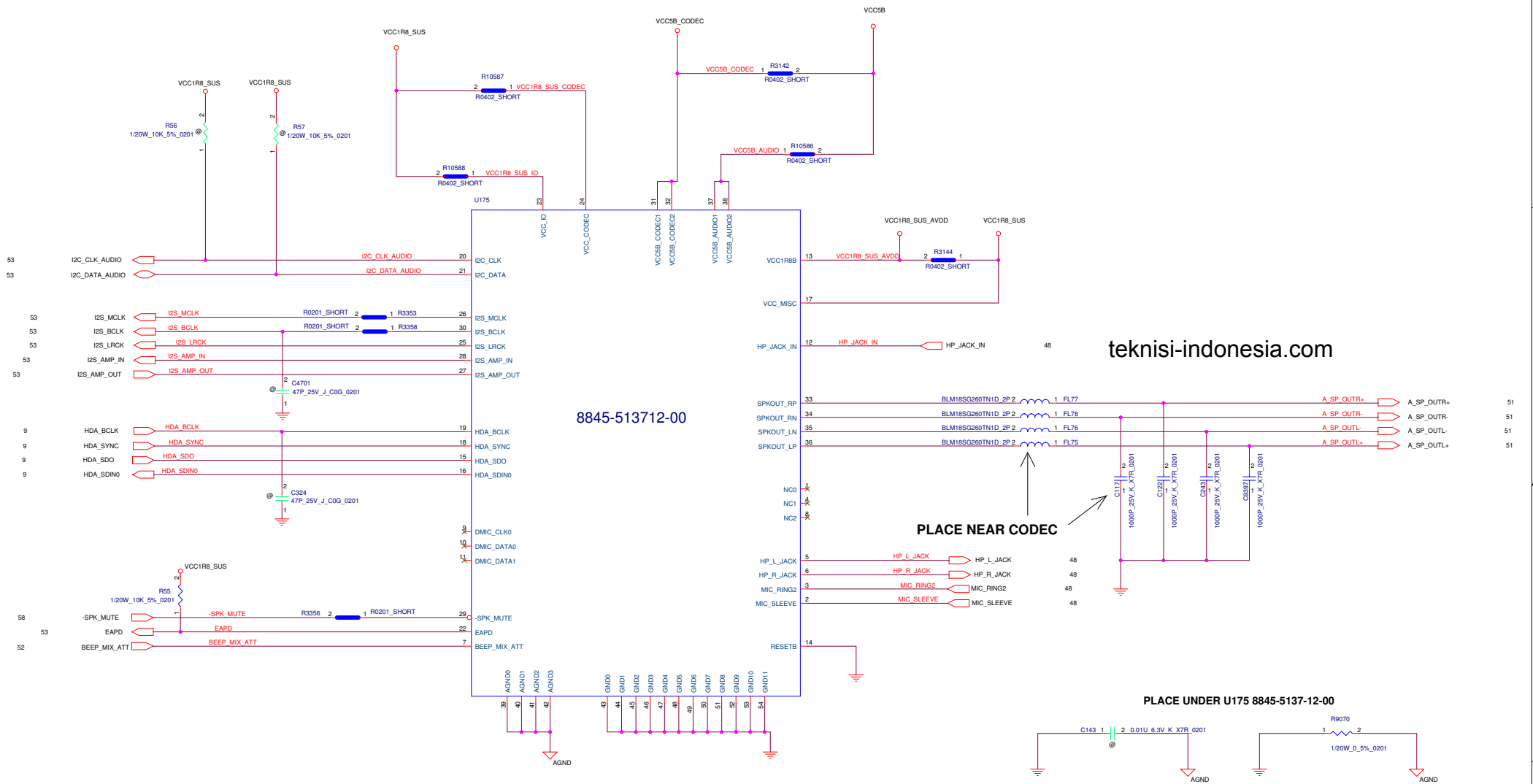
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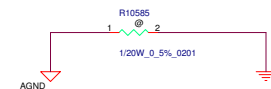
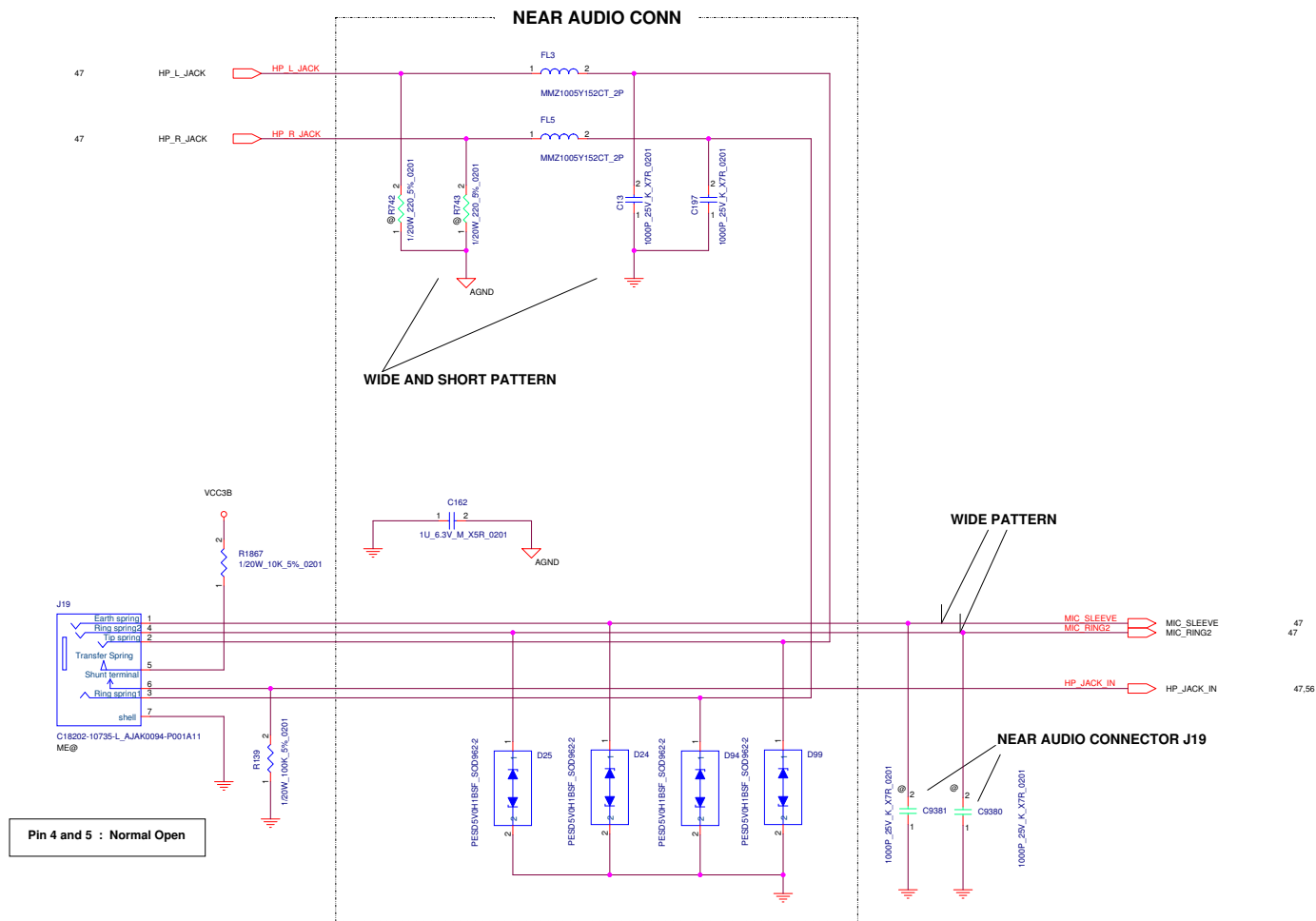
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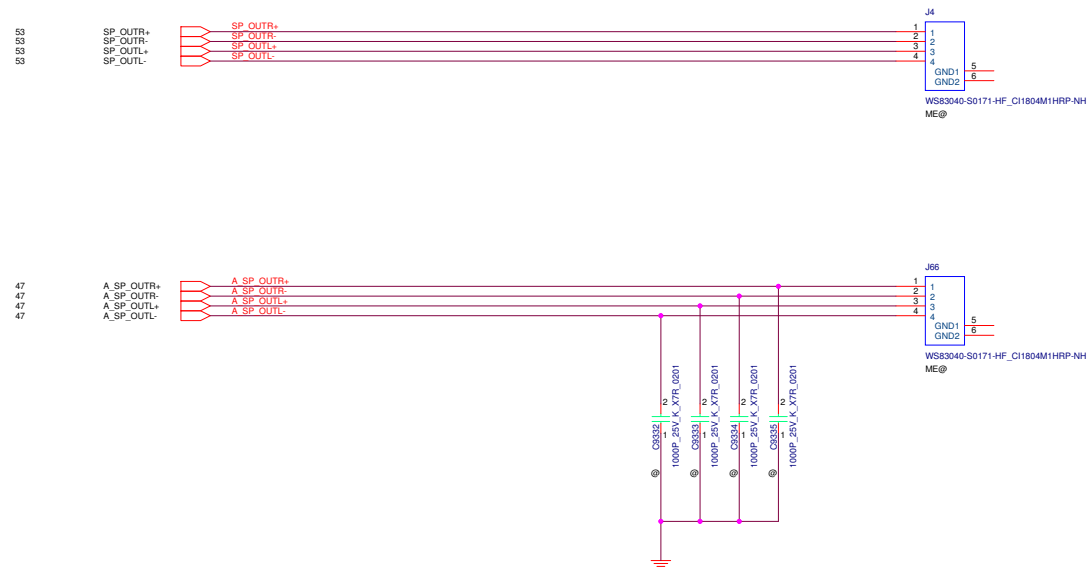


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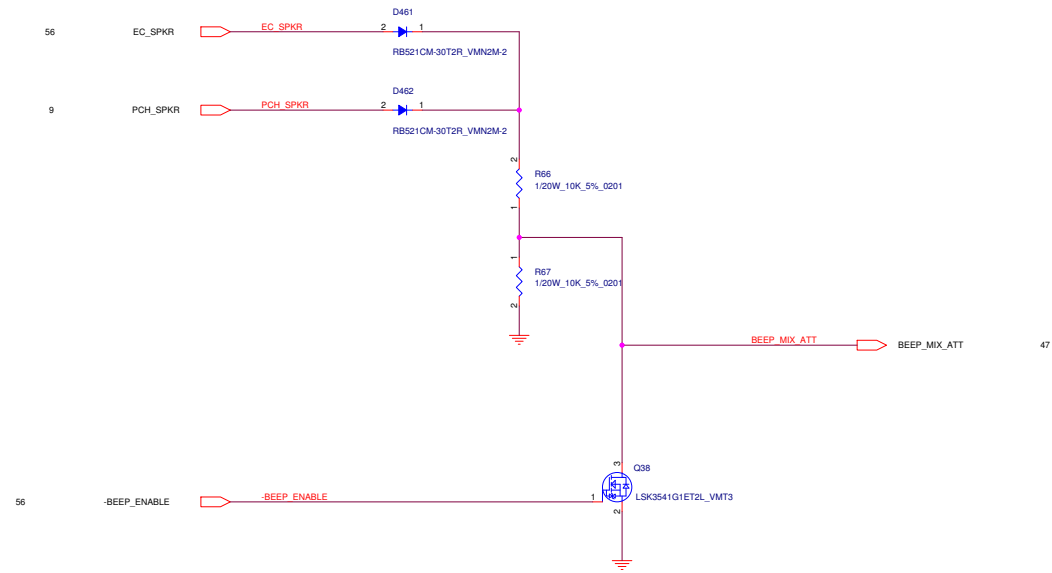
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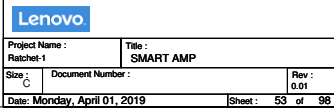
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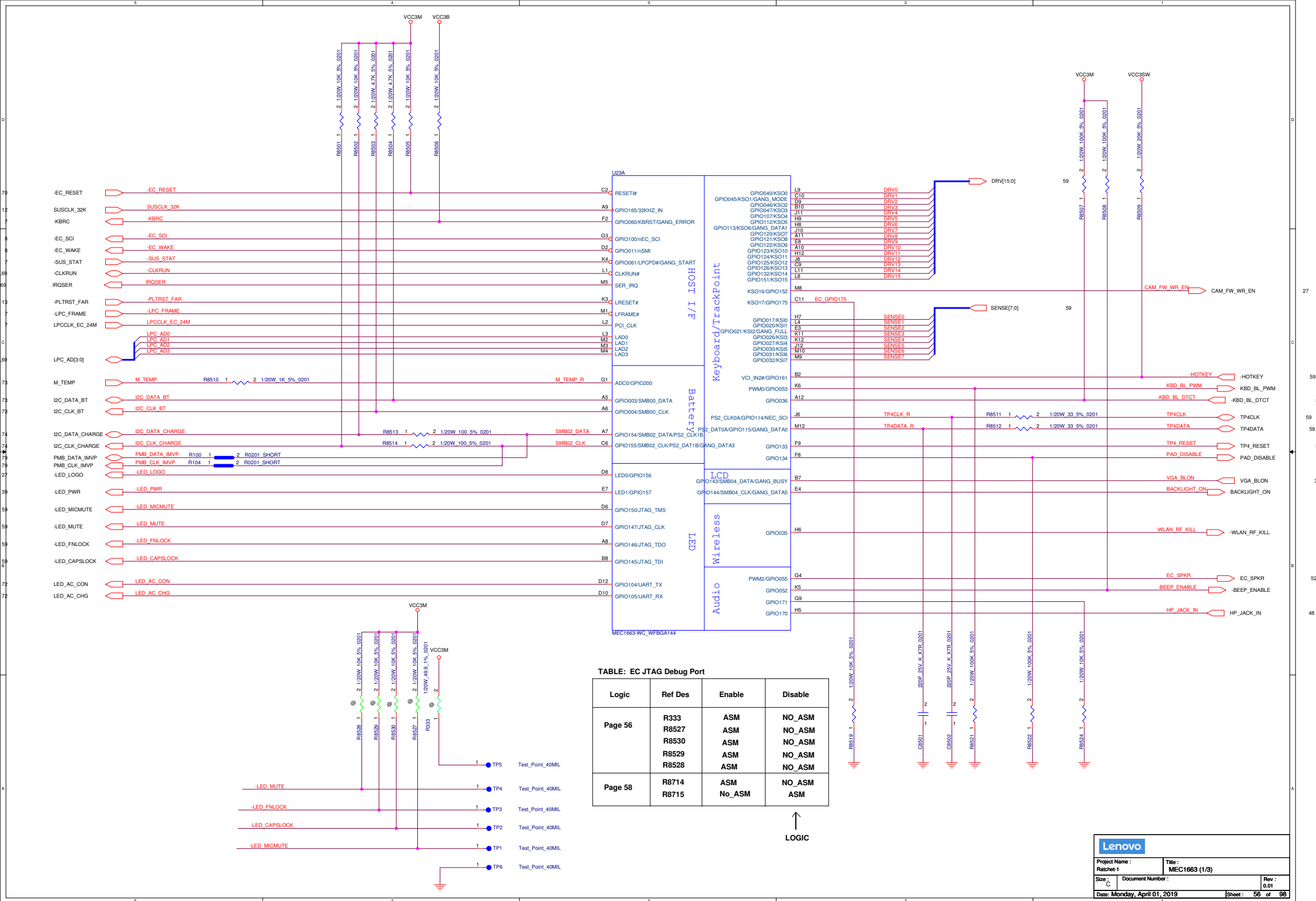


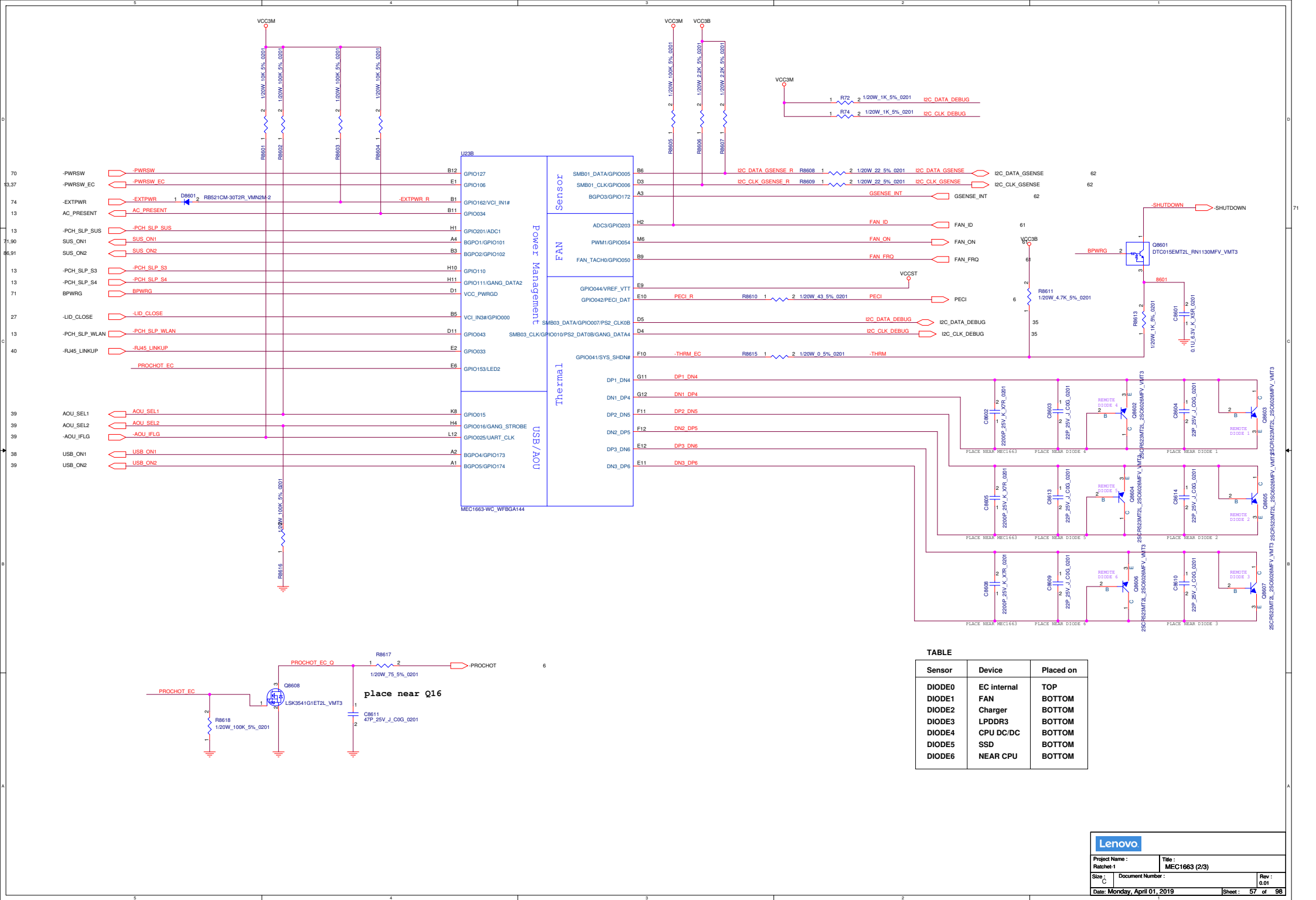
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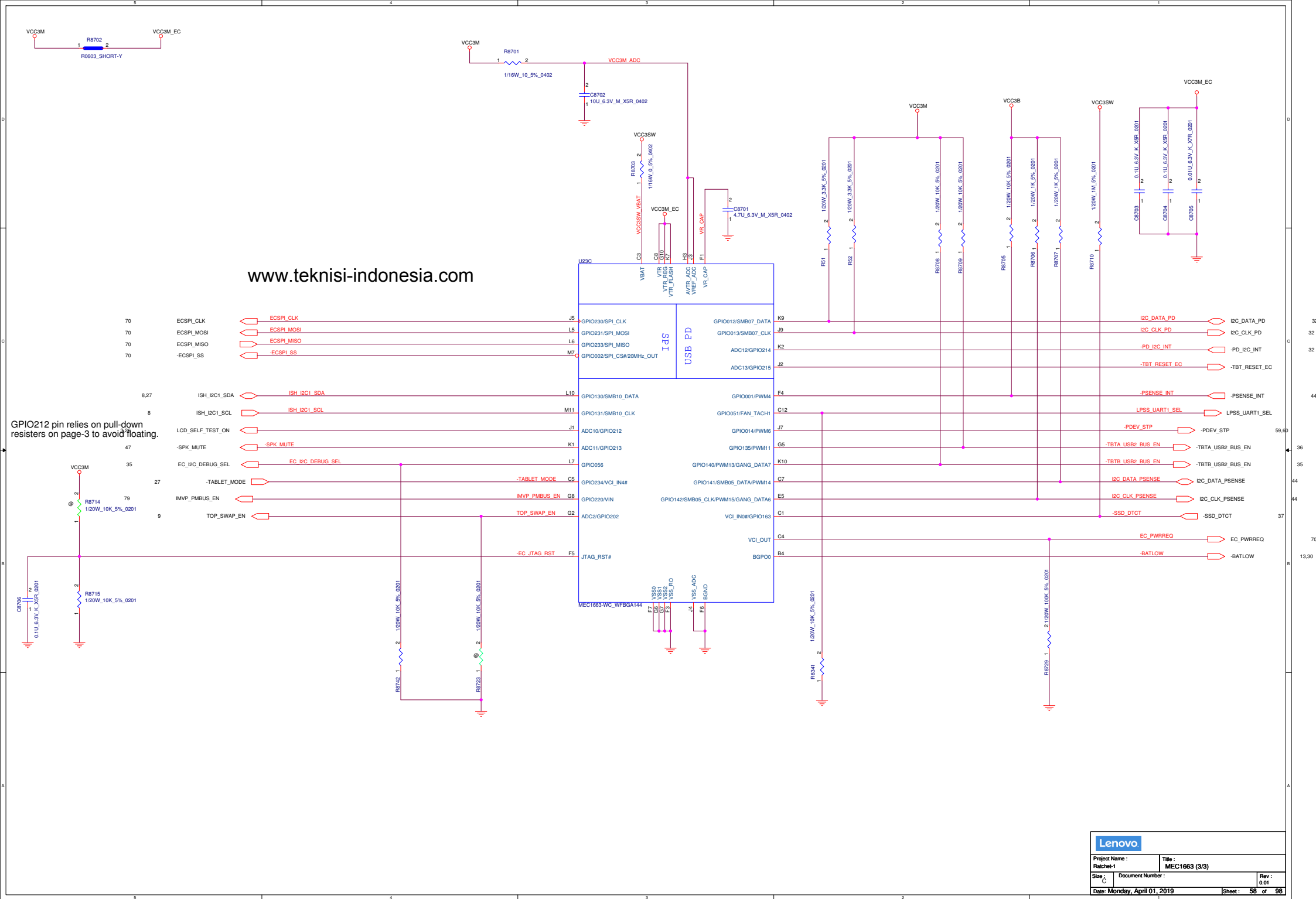
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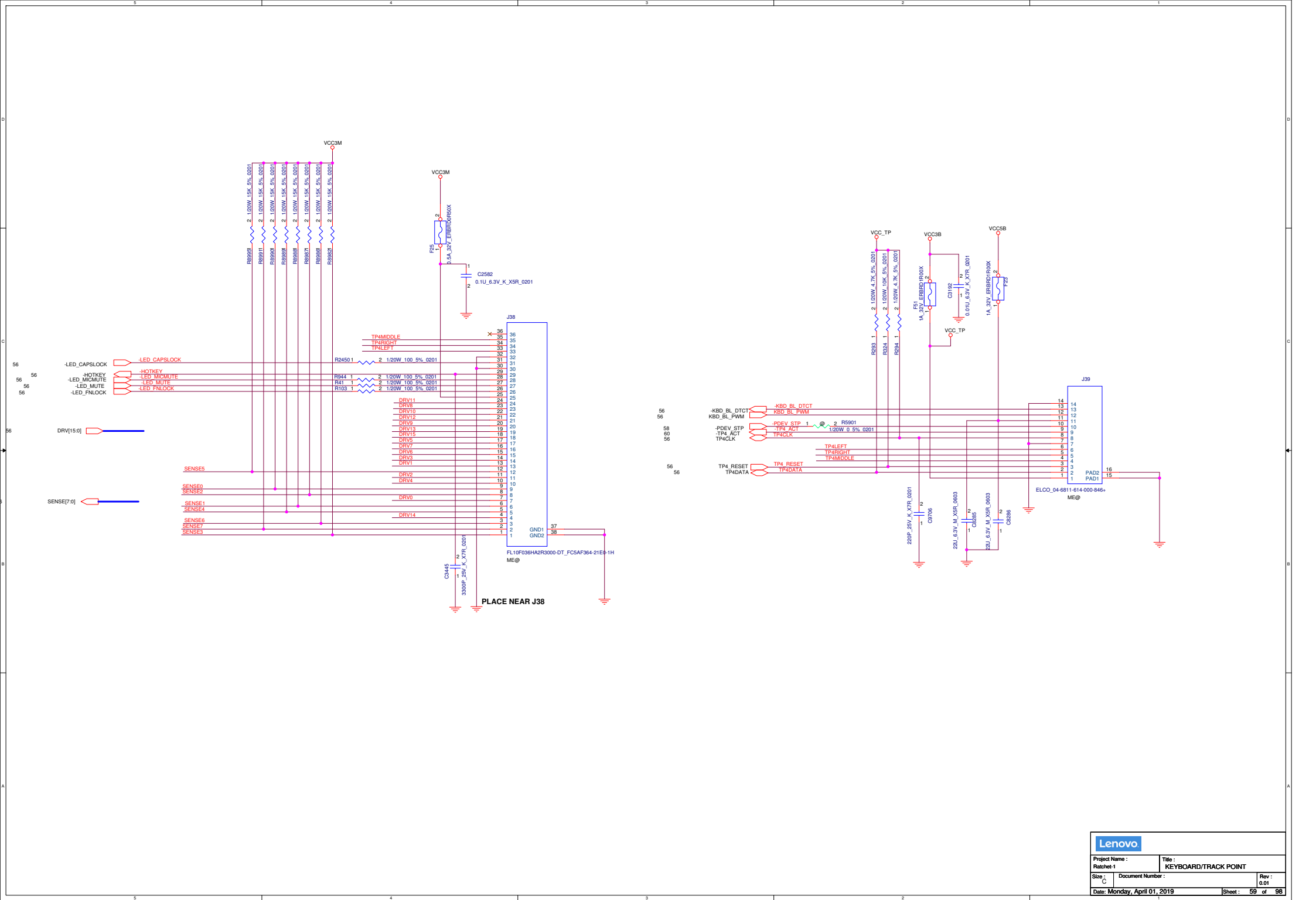


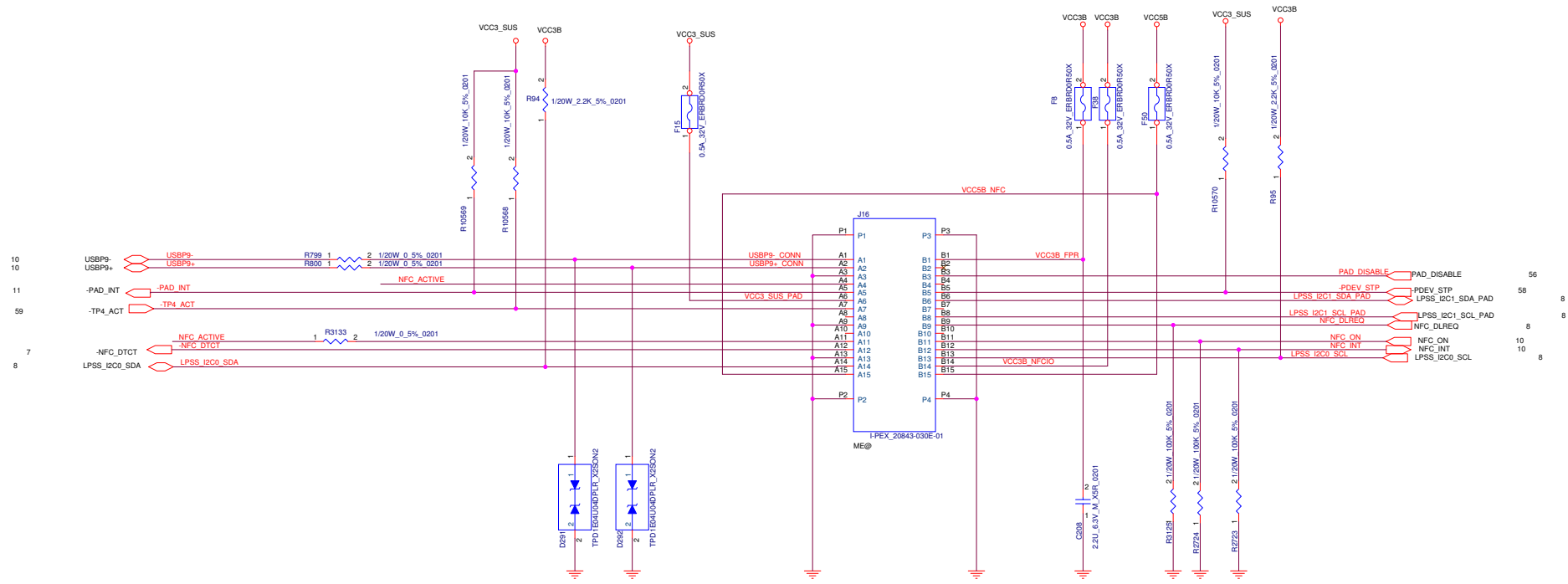


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GPIO12 pin relies on pull-down
resistors on page-3 to avoid floating.







PLACE NEAR J16

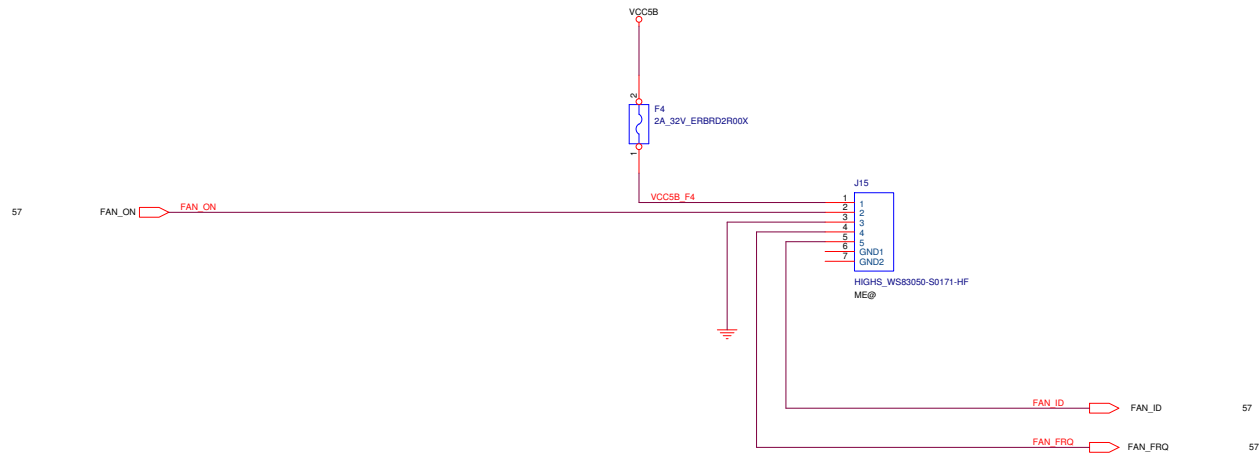
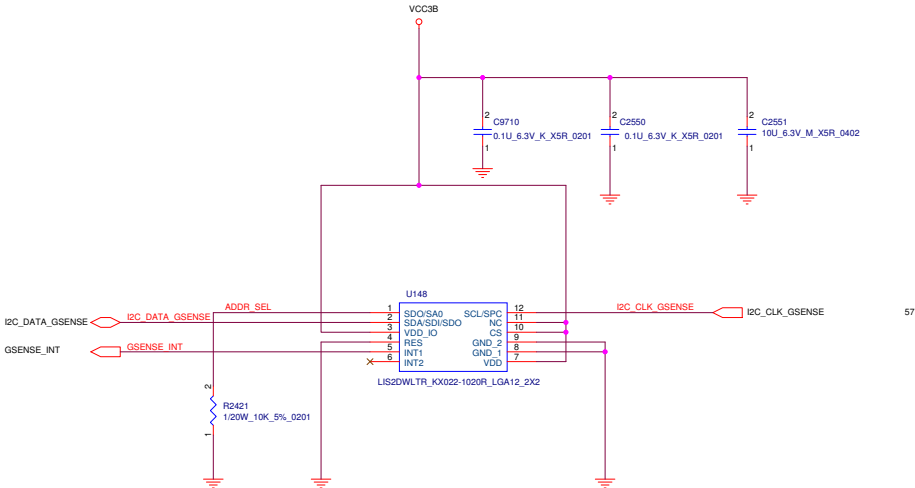


TABLE : G-Sensor Power

HDD Support	VCC3M
SSD Only	VCC3B

TABLE

P/N	ADDR_SEL	Address
LIS2DWL	H	32h (W) & 33h (R)
	L	30h (W) & 31h (R)
KX022-1020	H	3Eh (W) & 3Fh (R)
	L	3Ch (W) & 3Dh (R)



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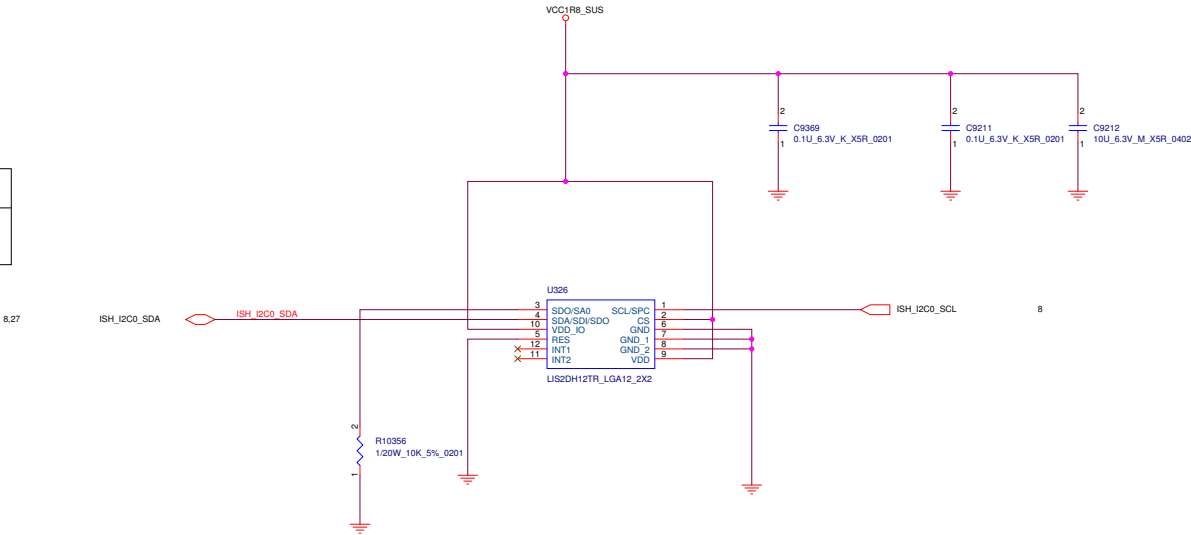
		
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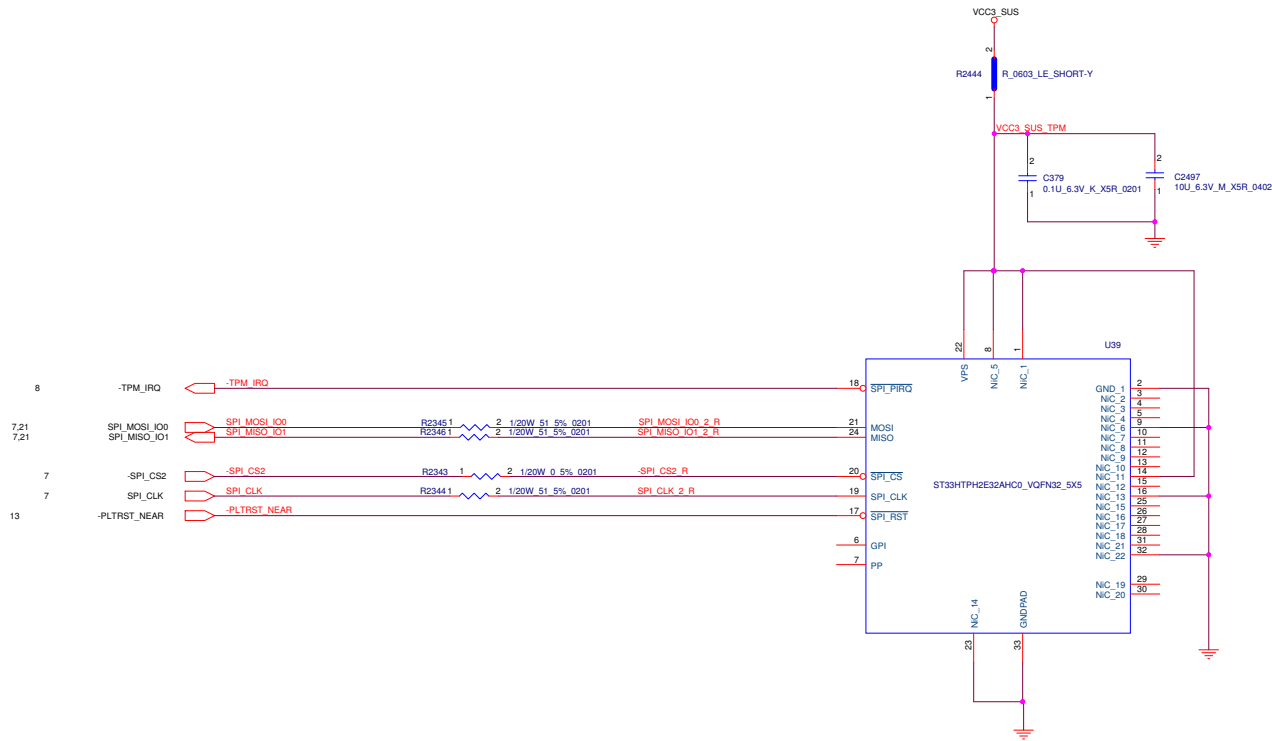
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Size : C	Document Number :	Rev : 0.01
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TABLE

P/N	ADDR_SEL	Address
LIS2DH12TR	H	31h (W) & 30h (R)
	L	33h (W) & 32h (R)





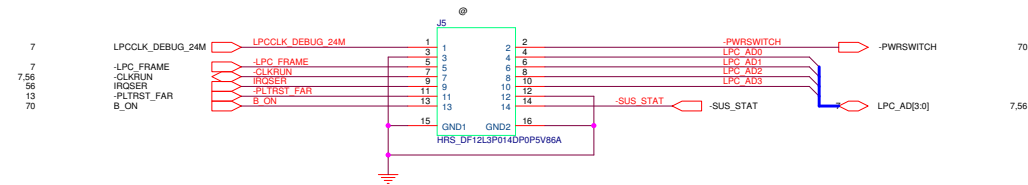
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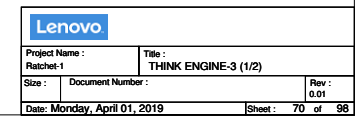
Pin No	TCG PTP Spec Rev.01.03.v22	ST Micro ST33HTPH2E32AH C0	Nuvoton NPCT750LABYX
1	VDD/VSB	NC	VSB
2	GND	GND	NC
3	GPIO	NC	NC
4	GPIO	NC	PP/GPIO6
5	NC	NC	NC
6	VNC/GPIO/I2C_PIRQ#	GPIO	GPIO3
7	GPIO/VDD	PP	NC
8	VDD	NC	VHIO
9	GND	NC	NC
10	VNC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	VNC/GPIO/I2C_PIRQ#	NC	GPIO4
14	VDD	NC	NC
15	NC	NC	NC
16	GND	NC	GND
17	SPI_RST#	SPI_RST#	PLTRST#
18	SPI_PIRQ#/I2C_PIRQ#	SPI_PIRQ#	PIRQ#/GPIO2
19	SPI_CLK	SPI_CLK	SCLK
20	SPI_CS#	SPI_CS#	SCS#/GPIO5
21	MOSI	MOSI	MOSI/GPIO7
22	VDD	VPS	VHIO
23	GND	NC	GND
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	VNC/GPIO	NC	NC
28	VNC/GPIO	NC	NC
29	SDA	NC	SDA/GPIO0
30	SCL	NC	SCL/GPIO1
31	VNC	NC	NC
32	GND	NC	NC

TABLE

REF DES	ENABLE	DISABLE
J5	ASM	NO_ASM
R220	ASM	NO_ASM

↑
LOGIC





ROHM: RB530CM-30
Toshiba: 1SS417

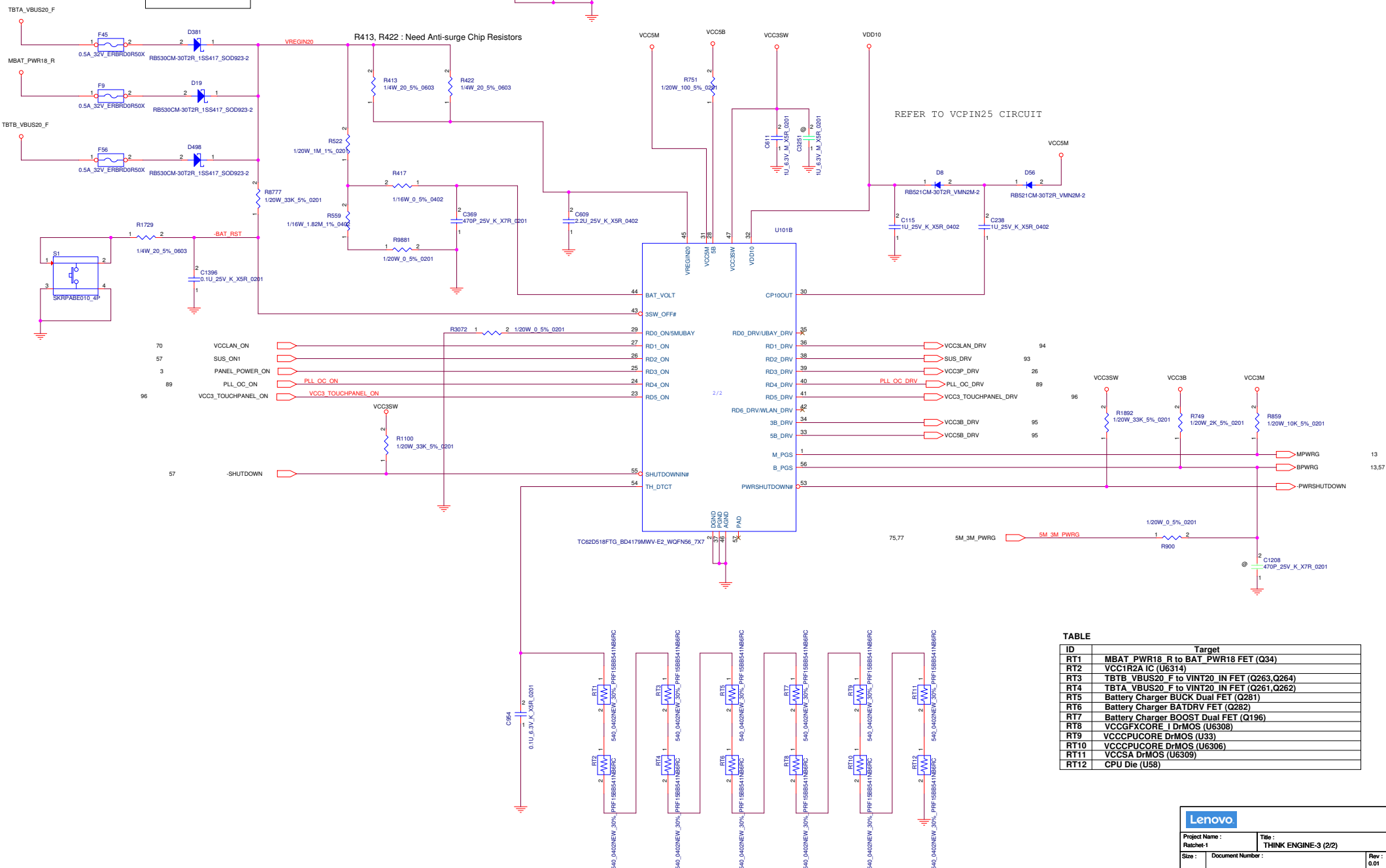


TABLE	
ID	Target
RT1	MBAT_PWR18 R to BAT_PWR18 FET (Q34)
RT2	VCC1R2A IC (U6314)
RT3	TB1T_VBUS20 F to VINT20 IN FET (Q263,Q264)
RT4	TB1T_VBUS20 F to VINT20 IN FET (Q261,Q262)
RT5	Battery Charger BUCK Dual FET (Q281)
RT6	Battery Charger BATDRV FET (Q282)
RT7	Battery Charger BOOST Dual FET (Q196)
RT8	VCCGFXCORE 1 DrMOS (U6308)
RT9	VCCPCUPCORE DrMOS (U33)
RT10	VCCPCUPCORE DrMOS (U6306)
RT11	VCCSA DrMOS (U6309)
RT12	CPU Die (U58)

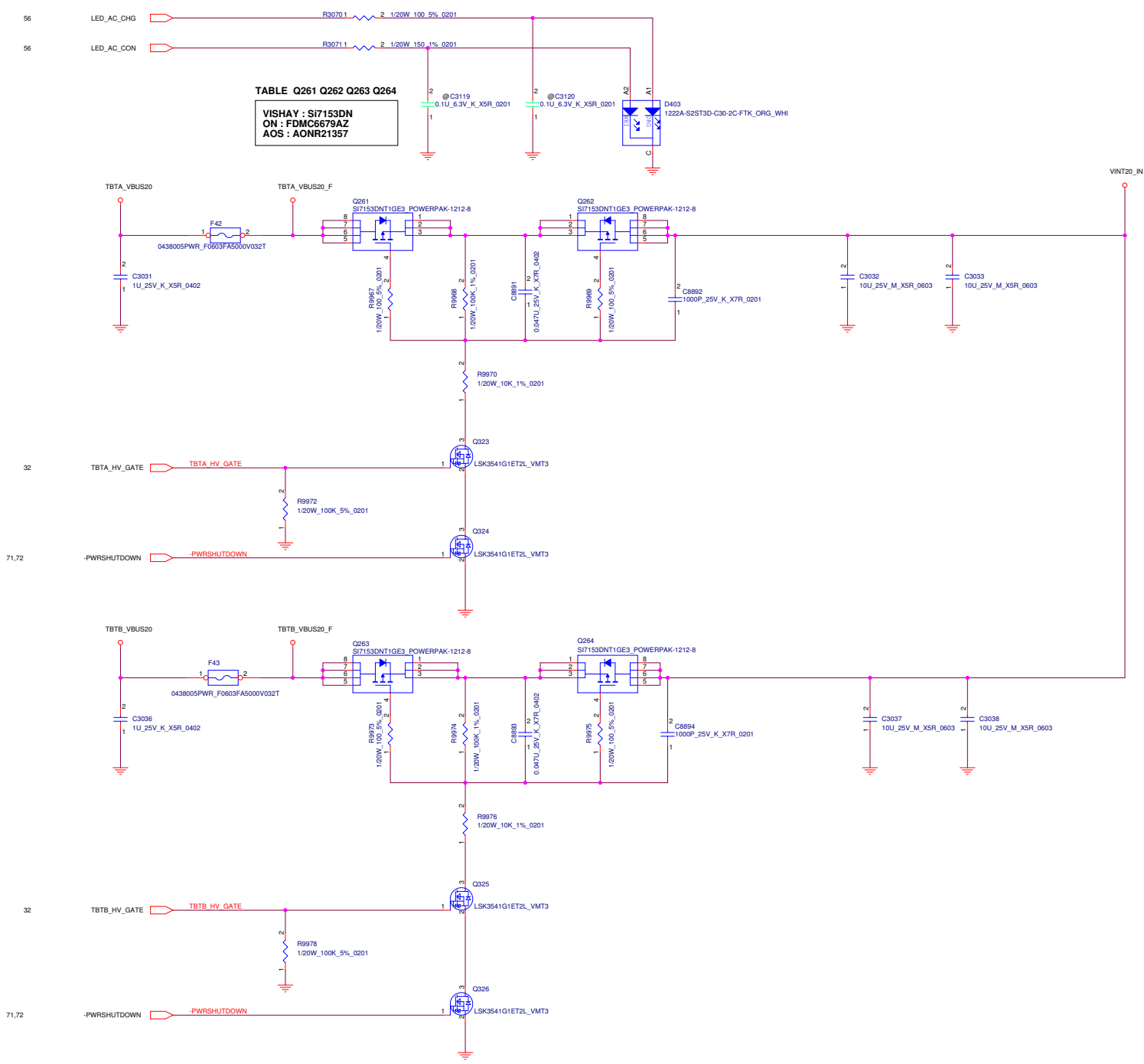


TABLE Q261 Q262 Q263 Q264
 VISHAY : Si7153DN
 ON : FDMC6679AZ
 AOS : AONR21357

VINT20_IN

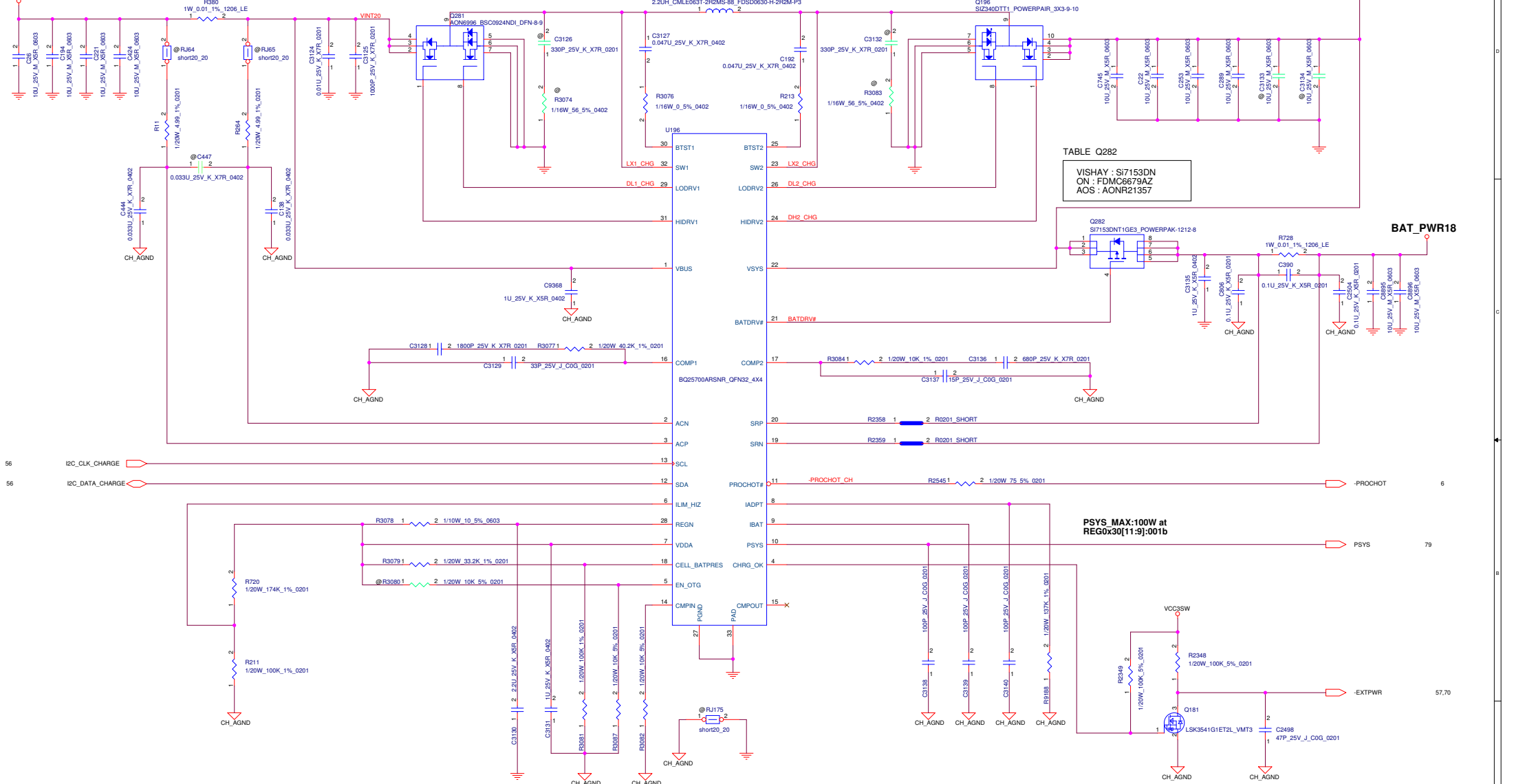


TABLE : ILIM_HIZ

IDPM	V (ILIM)	
500mA	1.2V	
1.0A	1.4V	
1.5A	1.6V	
2.0A	1.8V	237K
3.0A	2.2V	174K
3.25A	2.3V	162K

← LOGIC

TABLE : CELL_BATPRES

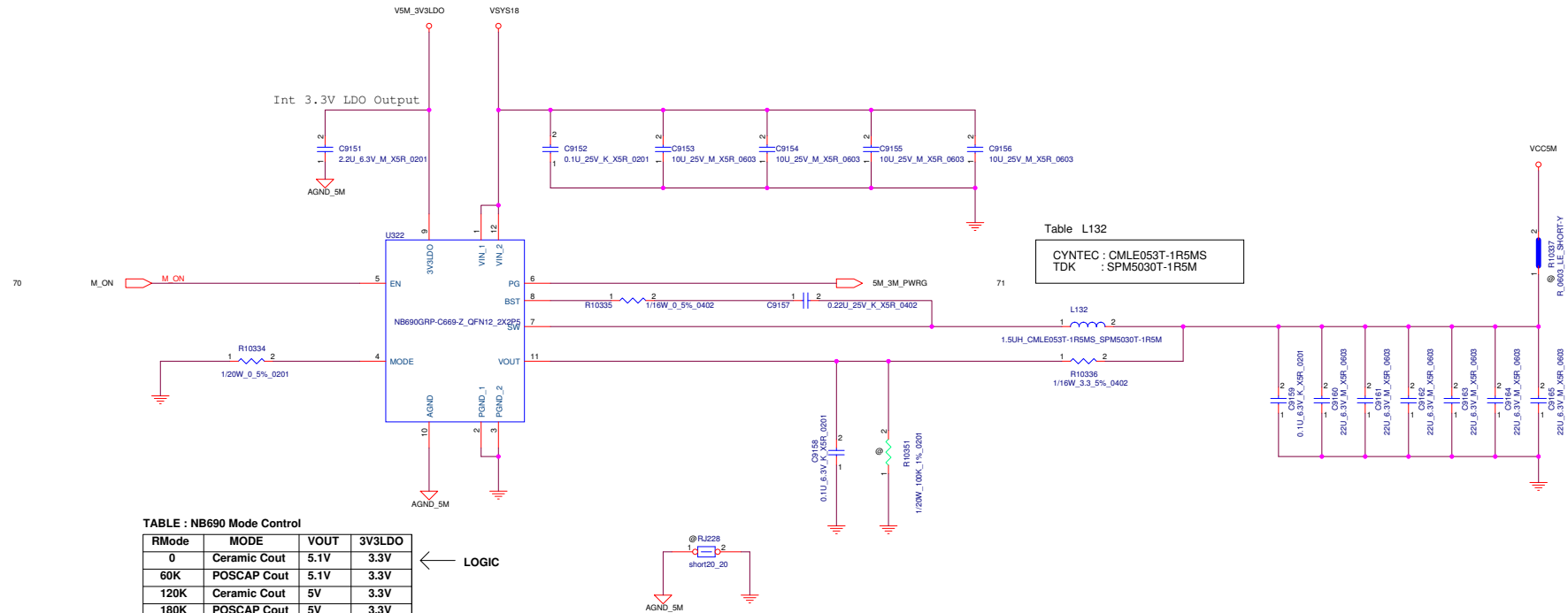
# of CELL	V (CELL_PRES)	R3079
1-CELL	1.5V	301K
2-CELL	2.5V	140K
3-CELL	3.5V	71.5K
4-CELL	4.5V	33.2K

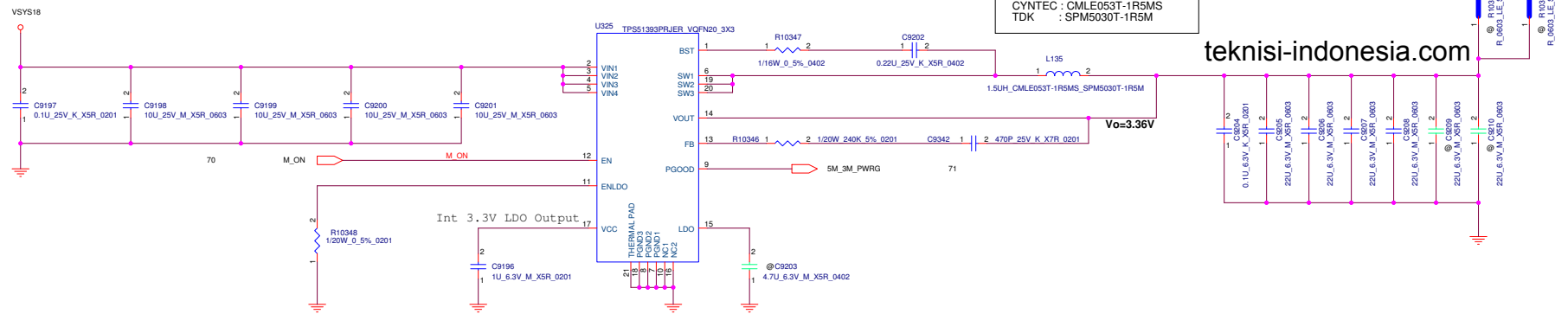
← LOGIC

TABLE

Inductor	R(IADP)	fsw@POR
1.0uH	93kohm	800kHz
2.2uH	137kohm	800kHz
3.3uH	169kohm	800kHz

← LOGIC





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VSYS18

VCC3M

PWM_CORE1

MODE_SEL

Table

SYNC (MODE_SEL)	
High	Normal Operation
H.Z.	Standby Mode
Low	Diode Emulation Mode

VSYS18

VCC3M

PWM_CORE2

MODE_SEL

VCCCPUCORE
U42
TDC= 48A
IccMax= 70A

TABLE L1603

CYNTEC
SUMIDA
CMLE062E-R15MS0R907-88
0624CDMCCDS-R15MC-D

VCCCPUCORE

TABLE R10659

ROHM: ESR03EZPJ1R0
PANASONIC: ERJPA3J1R0V

TABLE L1604

CYNTEC
SUMIDA
CMLE062E-R15MS0R907-88
0624CDMCCDS-R15MC-D

VCCCPUCORE

TABLE R10662

ROHM: ESR03EZPJ1R0
PANASONIC: ERJPA3J1R0V

2pcs 330uF + 25pcs for WHL U42 VCCCPUCORE


VCCCPUCORE

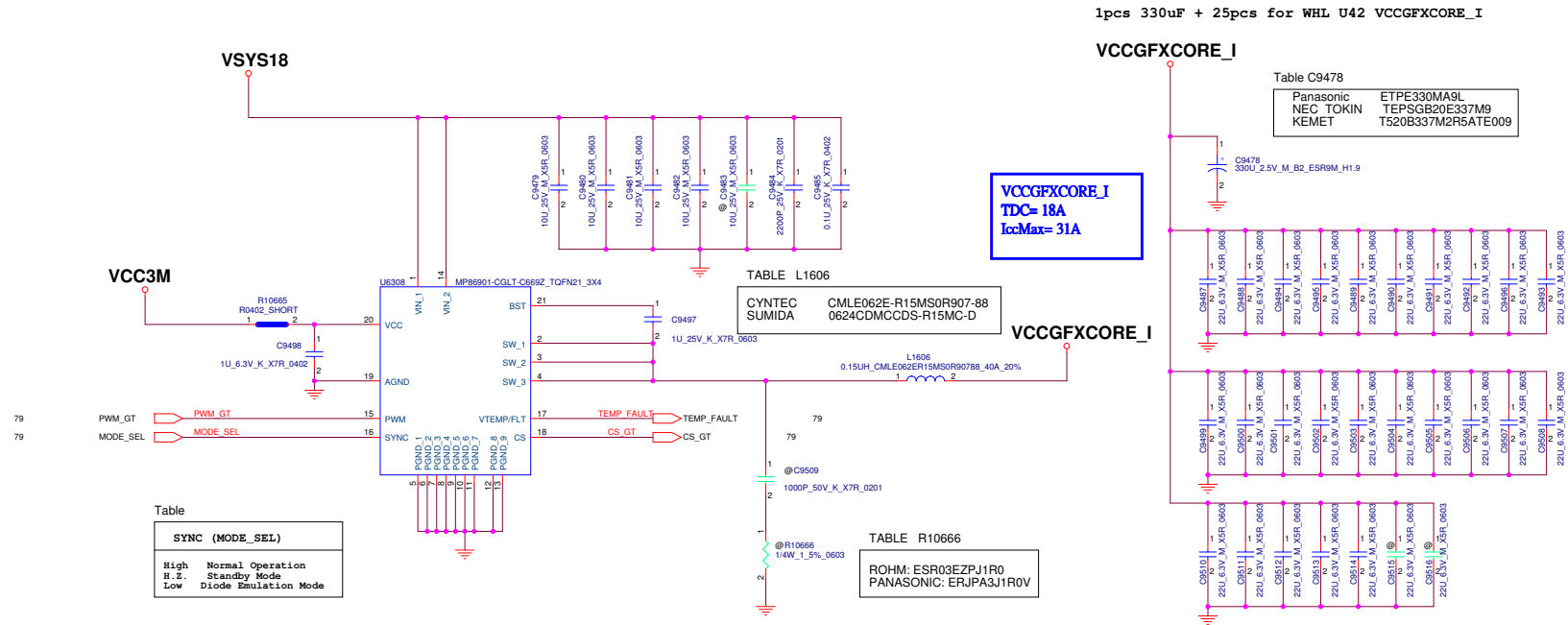
Table C9443,C9444

Panasonic ETPE330MA9L
NEC TOKIN TEPSGB20E337M9
KEMET T520B337M2R5A5TE009

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LP#	C1	C0	VOUT
0	X	X	0.000V
1	0	0	0.850V
1	0	1	0.875V
1	1	0	0.950V
1	1	1	0.975V

← LOGIC

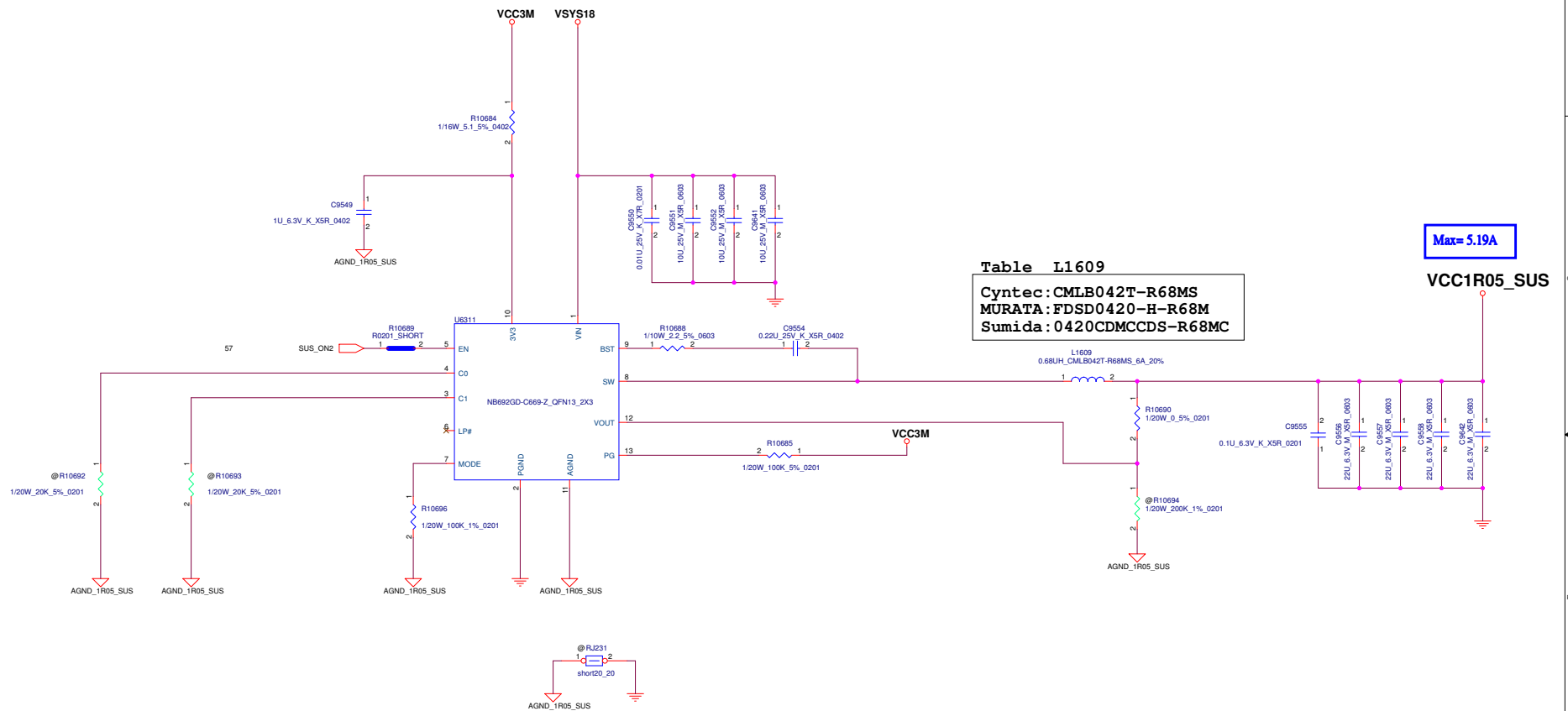


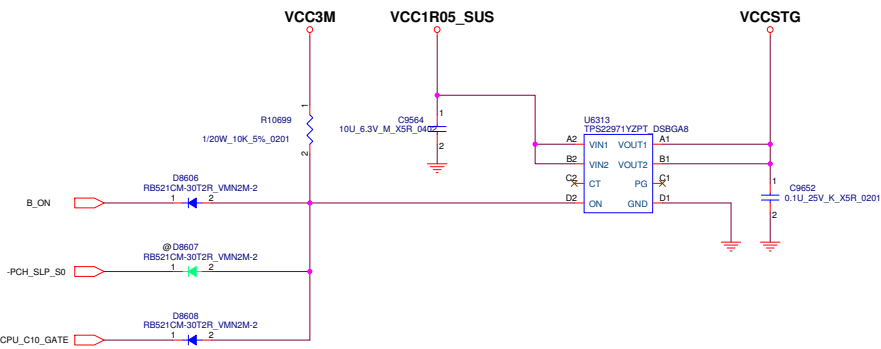
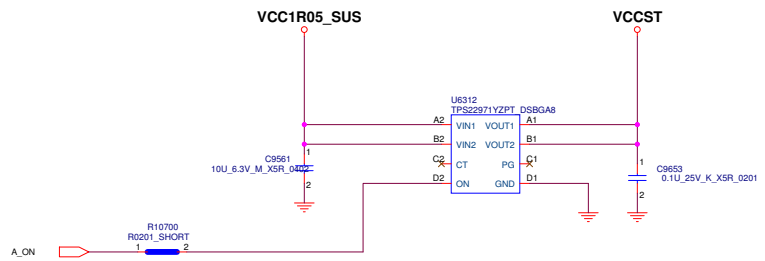
Table	L1609
Cyntec:	CMLB042T-R68MS
MURATA:	FDSD0420-H-R68M
Sumida:	0420CDMCCDS-R68MC

Max= 5.19A

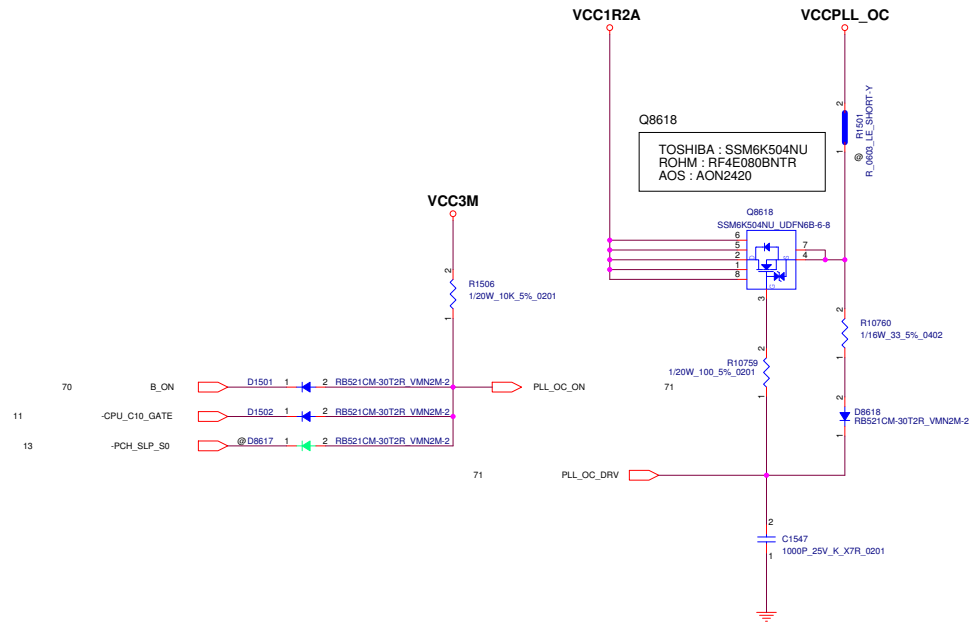
TABLE : NB692 MODE M3 (100Kohm to GND)

LP#	C1	C0	VOUT(V)
0	X	X	0V
1	0	0	0.8V
1	0	1	0.95V
1	1	0	1V
1	1	1	1.05V

← Default Value



$T_{on} < 65\mu s$



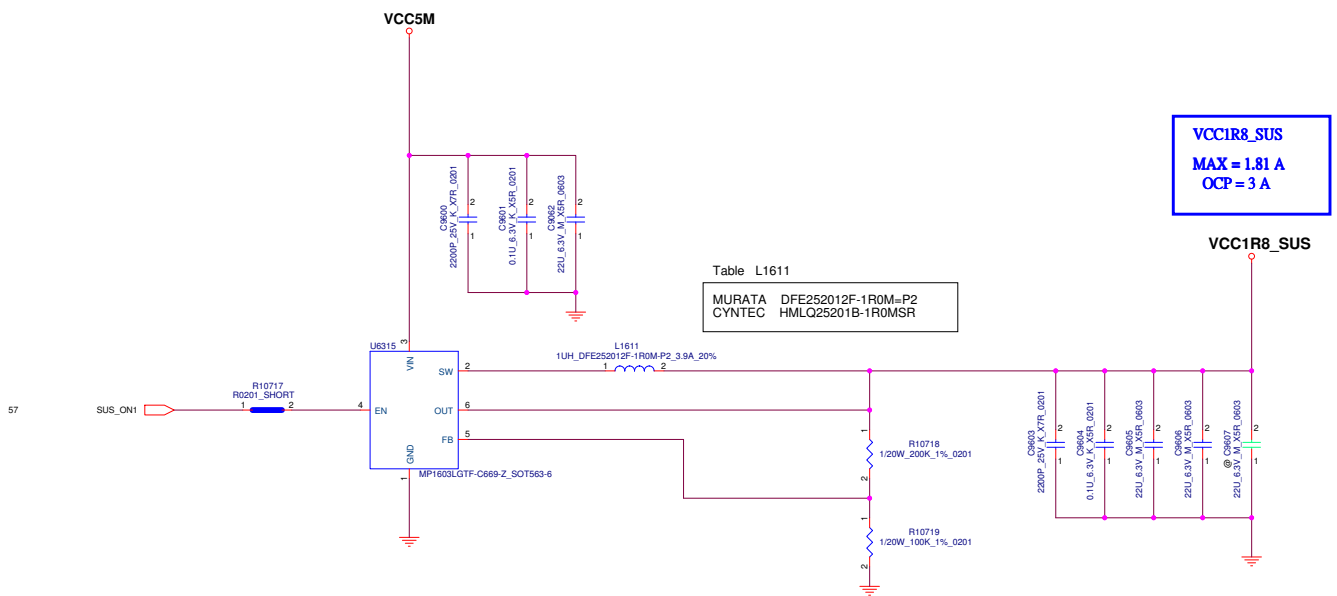


Table L1611

MURATA	DFE252012F-1R0M-P2
CYNTEC	HMLQ25201B-1R0MSR

VCC1R8_SUS
MAX = 1.81 A
OCP = 3 A

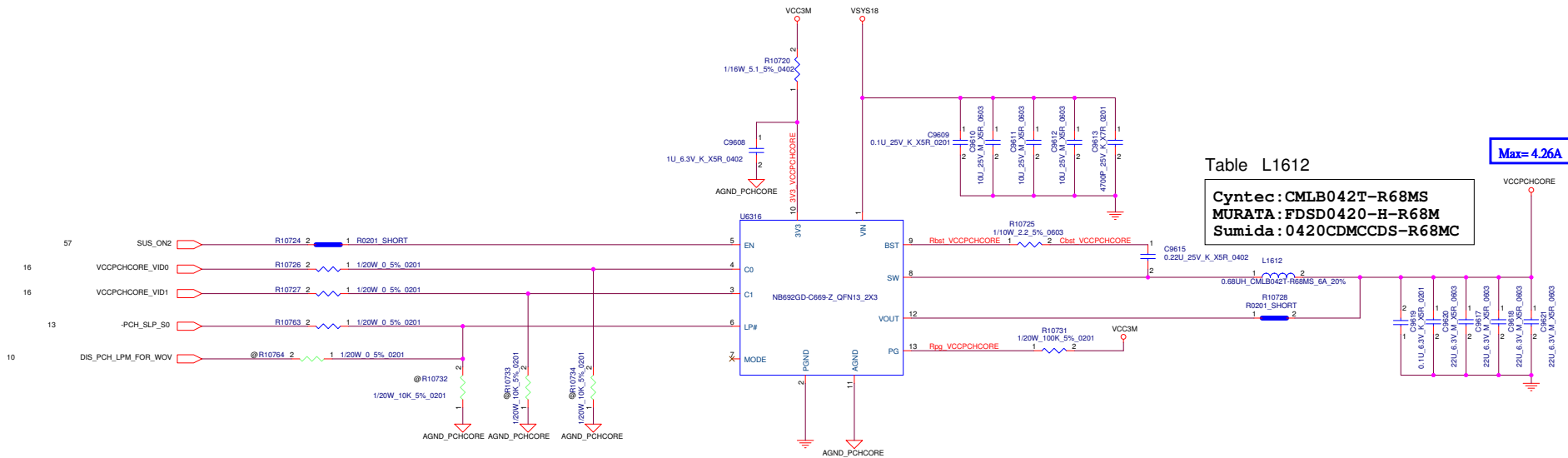


Table L1612

Cyntec: CMLB042T-R68MS
MURATA: FDSD0420-H-R68M
Sumida: 0420CDMCCDS-R68MC

Max= 4.26A

TABLE : NB692 MODE M2 (Float)

LP#	C1	C0	VOUT
0	X	X	0.75V
1	0	0	0.90V
1	0	1	0.95V
1	1	0	1.00V
1	1	1	1.05V

← SLP_S0#

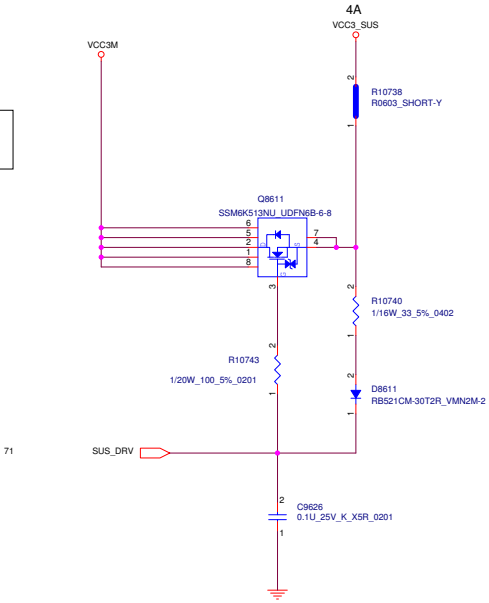
← DEFAULT

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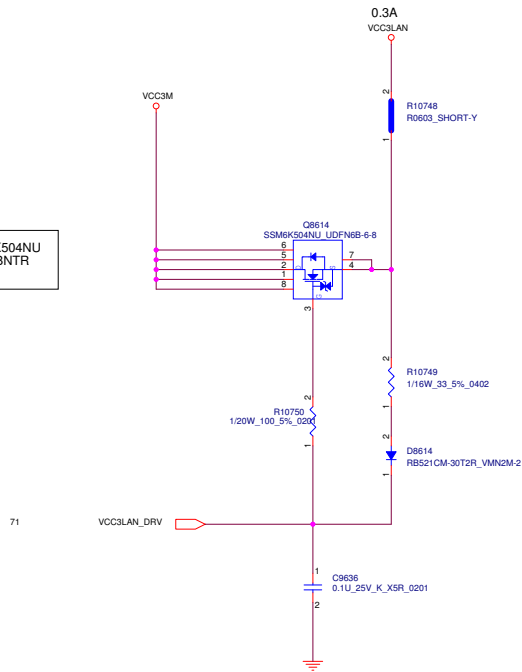
Lenovo		
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Q8611

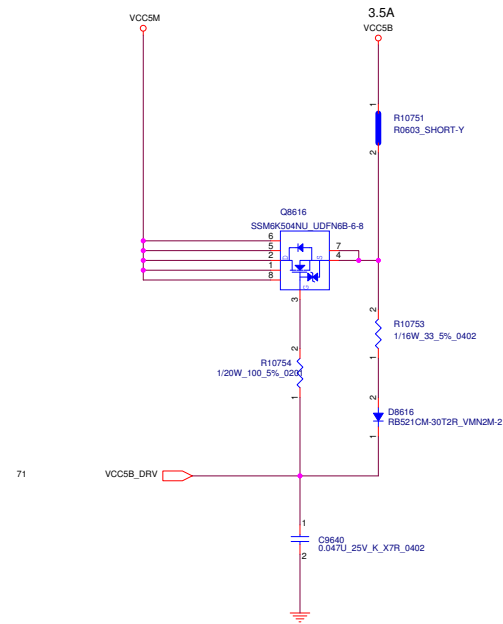
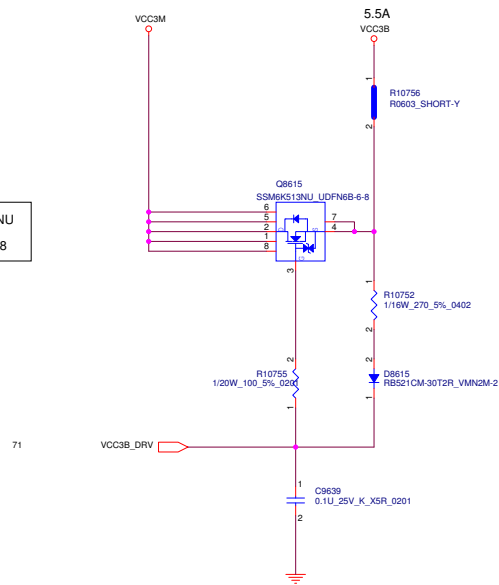
TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD : FDMA8878



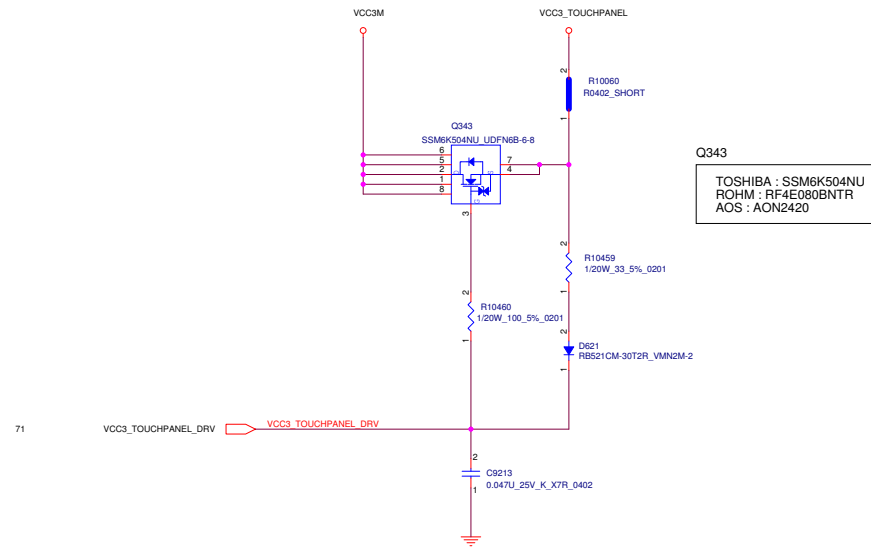
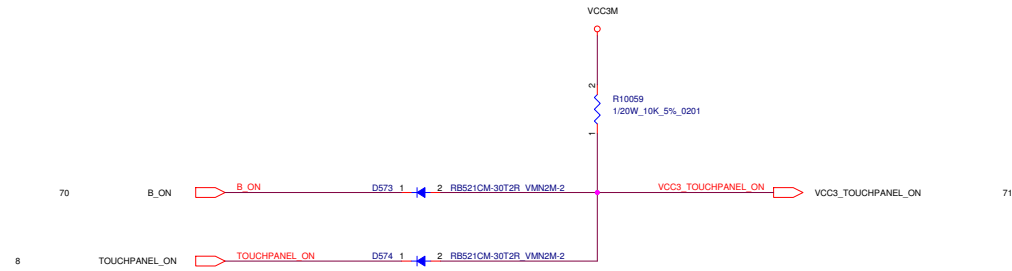
Q8614
TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420



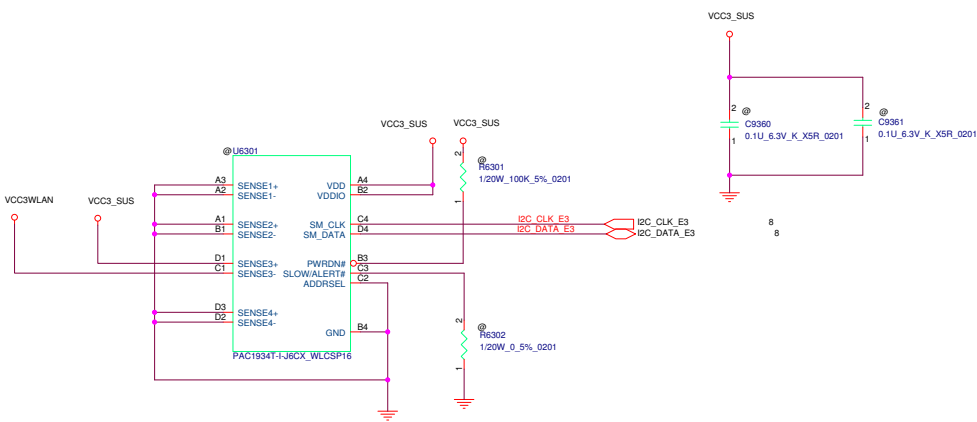
Q8615
TOSHIBA : SSM6K513NU
AOS : AON2420
FAIRCHILD : FDMA8878



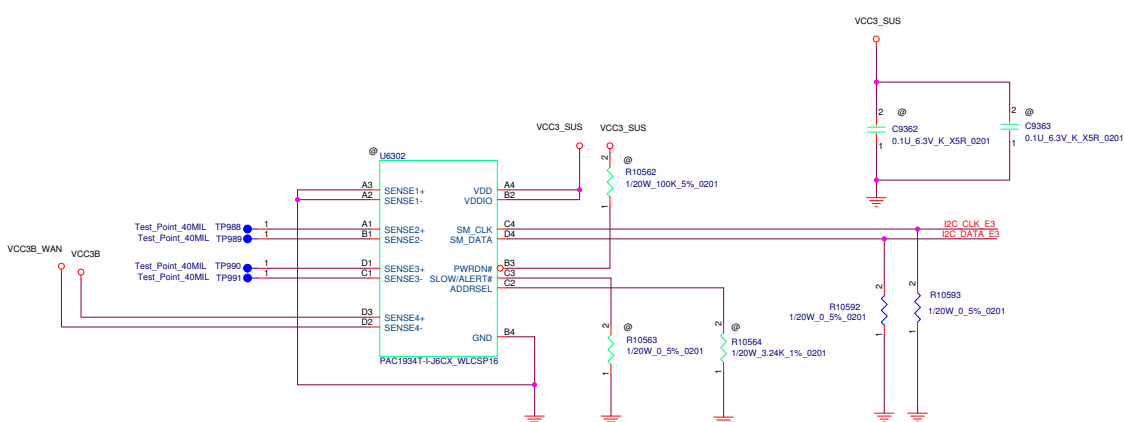
Q8616
TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420



Q343
TOSHIBA : SSM6K504NU
ROHM : RF4E080BNTR
AOS : AON2420

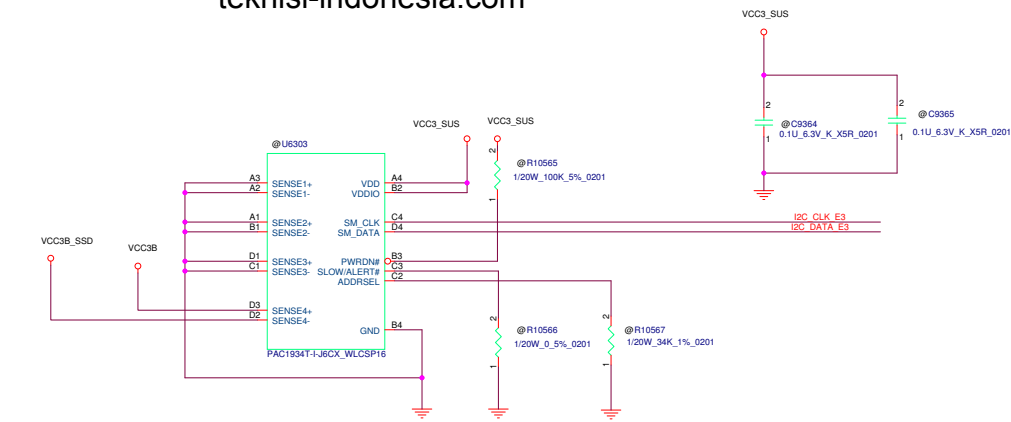


For WLAN I2C Address:0010_000 (ADDRSEL=0 (Tie to GND))

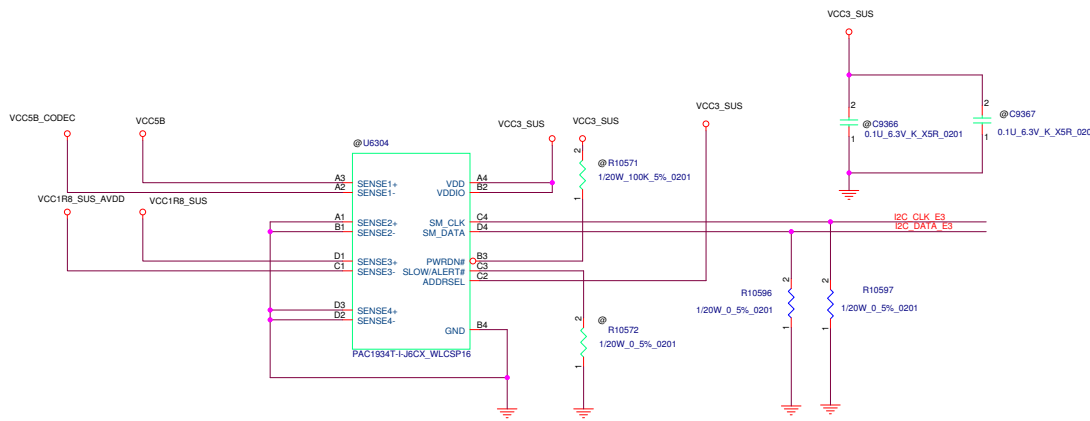


For WWAN I2C Address:0010_101 (ADDRSEL=3,240)

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For Storage I2C Address:0011_010 (ADDRSEL=34,000)



For Audio I2C Address:0011_111 (ADDRSEL=Tied to VDD)

FID
Board Area

